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Attorneys for Defendant
FREESCALE SEMICONDUCTOR, INC.

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

MAXIM INTEGRATED PRODUCTS,
INC.

Plaintiff,

v.

FREESCALE SEMICONDUCTOR, INC.

Defendant.

Case No. C 08-00979 MHP

**DEFENDANT FREESCALE
SEMICONDUCTOR, INC.'S ANSWER TO
AMENDED COMPLAINT FOR
DECLARATORY JUDGMENT AND
COUNTERCLAIMS**

DEMAND FOR JURY TRIAL

Defendant Freescale Semiconductor, Inc. (“Freescale”) responds to the Complaint for Declaratory Judgment by Plaintiff Maxim Integrated Products, Inc (“Maxim”) as follows:

PARTIES

1. Freescale is without knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 1 and, therefore, denies same.

2. Freescale admits the allegations in paragraph 2.

JURISDICTION AND VENUE

3. Freescale admits that this purports to be an action under the Declaratory Judgment Act, 28 U.S.C. §§ 2201 and 2202. Freescale denies all remaining allegations in paragraph 3.

4. Freescale admits that it owns the following patents (collectively, “the Freescale patents”):

U.S. Patent No. 5,089,722 (“the ’722 patent”) entitled “High speed output buffer circuit with overlap current control”;

U.S. Patent No. 5,105,250 (“the ’250 patent”) entitled “Heterojunction bipolar transistor with a thin silicon emitter”;

U.S. Patent No. 5,172,214 (“the ’214 patent”) entitled “Leadless semiconductor device and method for making the same”;

U.S. Patent No. 5,200, 362 (“the ’362 patent”) entitled “Method of attaching conductive traces to an encapsulated semiconductor die using a removable transfer film”;

U.S. Patent No. 5,434,739 (“the ’739 patent”) entitled “Reverse battery protection circuit”;

1 U.S. Patent No. 5,476,816 (“the ’816 patent”) entitled “Process for
2 etching an insulating layer after a metal etching step”; and

3 U.S. Patent No. 5,776,798 (“the ’798 patent”) entitled
4 “Semiconductor package and method thereof”;

5 5. Freescale admits that Maxim filed a declaratory judgment action in this Court
6 seeking a declaration that “the accused Maxim products and processes” have not infringed and
7 do not infringe “the asserted claims” of the Freescale patents and/or that these claims are invalid
8 and/or unenforceable, and denies the remaining allegations of paragraph 5.
9

10 6. Freescale admits that this Court has jurisdiction over this action under 28 U.S.C.
11 §§ 1331 and 1338(a), and denies the remaining allegations of paragraph 6.
12

13 7. Freescale admits that venue is proper, and denies the remaining allegations of
14 paragraph 7.

15 **INTRADISTRICT ASSIGNMENT**

16
17 8. The allegations of Paragraph 8 contain conclusions of law to which no response is
18 required.

19 **GENERAL ALLEGATIONS**

20
21 9. Freescale admits the allegations of paragraph 9.

22 10. Freescale admits the allegations of paragraph 10.

23 11. Freescale admits the allegations of paragraph 11.

24
25 12. Freescale admits that Maxim infringes some of its patents, that Maxim needs a
26 license to some of its patents, and that it met with Maxim via teleconference on August 8, 2007,
27
28

1 January 7, 2007 and in person on February 15, 2008. Freescale is without knowledge sufficient
2 to form a belief as to the truth of the remaining allegations in paragraph 12.

3 13. Freescale admits the allegations of paragraph 13.

4 14. Freescale denies the allegations of paragraph 14.

5 15. Freescale denies the allegations in paragraph 15.

6
7
8 **RESPONSE TO FIRST CLAIM**

9 **Declaratory Relief of the '722 Patent**

10 16. Freescale repeats and re-alleges paragraphs 1 through 15 as if fully set forth
11 herein.

12 17. Freescale denies the allegations in paragraph 17.

13
14 **RESPONSE TO SECOND CLAIM**

15 **Declaratory Relief of the '250 Patent**

16 18. Freescale repeats and re-alleges paragraphs 1 through 17 as if fully set forth
17 herein.

18 19. Freescale denies the allegations in paragraph 19.

19
20 **RESPONSE TO THIRD CLAIM**

21 **Declaratory Relief of the '214 Patent**

22 20. Freescale repeats and re-alleges paragraphs 1 through 19 as if fully set forth
23 herein.

24 21. Freescale denies the allegations in paragraph 21.

RESPONSE TO FOURTH CLAIM

Declaratory Relief of the '362 Patent

22. Freescale repeats and re-alleges paragraphs 1 through 21 as if fully set forth herein.

23. Freescale denies the allegations in paragraph 23.

RESPONSE TO FIFTH CLAIM

Declaratory Relief of the '739 Patent

24. Freescale repeats and re-alleges paragraphs 1 through 23 as if fully set forth herein.

25. Freescale denies the allegations in paragraph 25.

RESPONSE TO SIXTH CLAIM

Declaratory Relief of the '816 Patent

26. Freescale repeats and re-alleges paragraphs 1 through 25 as if fully set forth herein.

27. Freescale denies the allegations in paragraph 27. Freescale believes that Maxim infringes the '816 patent and plans to resort to discovery in this judicial process to confirm its belief, and if confirmed, will add a claim of infringement of the '816 patent by Maxim.

RESPONSE TO SEVENTH CLAIM

Declaratory Relief of the '798 Patent

28. Freescale repeats and re-alleges paragraphs 1 through 27 as if fully set forth herein.

29. Freescale denies the allegations in paragraph 29.

RESPONSE TO MAXIM'S "PRAYER FOR RELIEF"

Freescale denies that Maxim is entitled to any declaratory judgment relief.

Defendant Freescale Semiconductor, Inc. ("Freescale") responds to the Complaint for Declaratory Judgment by Plaintiff Maxim Integrated Products, Inc ("Maxim") as follows:

COUNTERCLAIMS

Freescale asserts as follows:

PARTIES

30. Upon information and belief, Maxim is a corporation organized and existing under the laws of the state of Delaware, with its principal place of business at 120 San Gabriel Drive, Sunnyvale, California 94086, which does business in this District and elsewhere in the State of California.

31. Freescale is a corporation organized and existing under the laws of Delaware, with its principal place of business at 6501 William Cannon Drive West, Austin, Texas 78735.

JURISDICTION AND VENUE

32. This is an action for patent infringement under the Patent Laws of the United States, 35 U.S.C. § 271.

33. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

34. Maxim does business in this State and District and has sufficient contacts to subject it to the personal jurisdiction of this Court for this patent infringement action. Maxim

1 has placed its products and services, including infringing products and services, into the stream
2 of commerce, knowing or reasonably expecting that such products will be used, sold, or offered
3 to be sold in this State and in this District.

4
5 35. Venue is proper in this district under 28 U.S.C. §§ 1391(b)-(c), and 1400(b).

6
7
8 **GENERAL ALLEGATIONS**

9 36. On February 18, 1992, the United States Patent and Trademark Office
10 (“USPTO”) duly and legally issued United States Patent No. 5,089,722 entitled “High speed
11 output buffer circuit with overlap current control” to Motorola, Inc. as the assignee of inventor
12 Robert J. Amedeo (“the ’722 patent”). The ’722 patent was subsequently assigned to Freescale
13 Semiconductor, Inc. Freescale is the sole and exclusive owner of the entire right, title, and
14 interest in and to the ’722 patent. A copy of the ’722 patent is attached as Exhibit A.

15 37. On April 14, 1992, the USPTO duly and legally issued United States Patent No.
16 5,105,250 entitled “Heterojunction bipolar transistor with a thin silicon emitter” to Motorola, Inc.
17 as the assignee of inventors Gordon Tam and Lynnita K. Knoch (“the ’250 patent”). The ’250
18 patent was subsequently assigned to Freescale Semiconductor, Inc. Freescale is the sole and
19 exclusive owner of the entire right, title, and interest in and to the ’250 patent. A copy of the
20 ’250 patent is attached as Exhibit B.

21
22 38. On December 15, 1992, the USPTO duly and legally issued United States Patent
23 No. 5,172,214 entitled “Leadless semiconductor device and method for making the same” to
24 Motorola, Inc. as the assignee of inventor James J. Casto (“the ’214 patent”). The ’214 patent
25 was subsequently assigned to Freescale Semiconductor, Inc. Freescale is the sole and exclusive
26
27
28

owner of the entire right, title, and interest in and to the '214 patent. A copy of the '214 patent is attached as Exhibit C.

39. On April 6, 1993, the USPTO duly and legally issued United States Patent No. 5,200,362 entitled "Method of attaching conductive traces to an encapsulated semiconductor die using a removable transfer film" to Motorola, Inc. as the assignee of inventors Paul T. Lin, Michael B. McShane, Sugio Uchida, and Takehi Sato ("the '362 patent"). The '362 patent was subsequently assigned to Freescale Semiconductor, Inc. Freescale is the sole and exclusive owner of the entire right, title, and interest in and to the '362 patent. A copy of the '362 patent is attached as Exhibit D.

40. On July 18, 1995, the USPTO duly and legally issued United States Patent No. 5,434,739 entitled "Reverse battery protection circuit" to Motorola, Inc. as the assignee of inventor Karl R. Heck ("the '739 patent"). The '739 patent was subsequently assigned to Freescale Semiconductor, Inc. Freescale is the sole and exclusive owner of the entire right, title, and interest in and to the '739 patent. A copy of the '739 patent is attached as Exhibit E

41. On July 7, 1998, the USPTO duly and legally issued United States Patent No. 5,776,798 entitled "Semiconductor package and method thereof" to Motorola, Inc. as the assignee of inventors Son Ky Quan, Samuel L. Coffman, Bruce Reid, Keith E. Nelson, and Deborah A. Hagen ("the '798 patent"). The '798 patent was subsequently assigned to Freescale Semiconductor, Inc. Freescale is the sole and exclusive owner of the entire right, title, and interest in and to the '798 patent. A copy of the '798 patent is attached as Exhibit F.

42. Maxim has been for some time past and is presently infringing the counterclaim Freescale patents within this District and elsewhere in this country by manufacturing, selling, offering for sale, and using semiconductor devices embodying the patented inventions of the

1 counterclaim Freescale patents, and will continue to do so, and will continue unless enjoined by
2 this Court.

3 **FIRST CLAIM FOR RELIEF**

4 **Infringement of the '722 Patent**

5
6 43. Freescale repeats and re-alleges paragraphs 30 through 42 as if fully set forth
7 herein.

8
9 44. Maxim has been and is now directly infringing, and indirectly infringing by way
10 of inducing infringement and/or contributing to the infringement, on Freescale's '722 patent in
11 this District and elsewhere by, making, using, offering for sale, selling, or importing products
12 and/or processes covered by at least one claim of the '722 patent, all to the injury of Freescale.

13 45. At relevant times, Freescale provided actual notice of the '722 patent to Maxim in
14 accordance with 35 U.S.C. § 287.

15
16 46. Upon information and belief, Maxim had and has actual notice of the '722 patent,
17 Maxim has been and is aware of its infringement, and Maxim's infringement has been and
18 continues to be willful.

19
20 47. Freescale has been damaged by Maxim's infringement of the '722 patent and will
21 continue to be damaged in the future unless Maxim is permanently enjoined from infringing the
22 '722 patent.

23 **SECOND CLAIM FOR RELIEF**

24 **Infringement of the '250 Patent**

25
26 48. Freescale repeats and re-alleges paragraphs 30 through 42 as if fully set forth
27 herein.

49. Maxim has been and is now directly infringing, and indirectly infringing by way of inducing infringement and/or contributing to the infringement, on Freescale's '250 patent in this District and elsewhere by, making, using, offering for sale, selling, or importing products and/or processes covered by at least one claim of the '250 patent, all to the injury of Freescale.

50. At relevant times, Freescale provided actual notice of the '250 patent to Maxim in accordance with 35 U.S.C. § 287.

51. Upon information and belief, Maxim had and has actual notice of the '250 patent, Maxim has been and is aware of its infringement, and Maxim's infringement has been and continues to be willful.

52. Freescale has been damaged by Maxim's infringement of the '250 patent and will continue to be damaged in the future unless Maxim is permanently enjoined from infringing the '250 patent.

THIRD CLAIM FOR RELIEF

Infringement of the '214 Patent

53. Freescale repeats and re-alleges paragraphs 30 through 42 as if fully set forth herein.

54. Maxim has been and is now directly infringing, and indirectly infringing by way of inducing infringement and/or contributing to the infringement, on Freescale's '214 patent in this District and elsewhere by, making, using, offering for sale, selling, or importing products and/or processes covered by at least one claim of the '214 patent, all to the injury of Freescale.

55. At relevant times, Freescale provided actual notice of the '214 patent to Maxim in accordance with 35 U.S.C. § 287.

57. Freescale has been damaged by Maxim's infringement of the '214 patent and will continue to be damaged in the future unless Maxim is permanently enjoined from infringing the '214 patent.

Infringement of the '362 Patent

59. Maxim has been and is now directly infringing, and indirectly infringing by way of inducing infringement and/or contributing to the infringement, on Freescale's '362 patent in this District and elsewhere by, making, using, offering for sale, selling, or importing products and/or processes covered by at least one claim of the '362 patent, all to the injury of Freescale.

61. Upon information and belief, Maxim had and has actual notice of the '362 patent, Maxim has been and is aware of its infringement, and Maxim's infringement has been and continues to be willful.

62. Freescale has been damaged by Maxim's infringement of the '362 patent and will continue to be damaged in the future unless Maxim is permanently enjoined from infringing the '362 patent.

FIFTH CLAIM FOR RELIEF**Infringement of the '739 Patent**

63. Freescale repeats and re-alleges paragraphs 30 through 42 as if fully set forth herein.

64. Maxim has been and is now directly infringing, and indirectly infringing by way of inducing infringement and/or contributing to the infringement, on Freescale's '739 patent in this District and elsewhere by, making, using, offering for sale, selling, or importing products and/or processes covered by at least one claim of the '739 patent, all to the injury of Freescale.

65. At relevant times, Freescale provided actual notice of the '739 patent to Maxim in accordance with 35 U.S.C. § 287.

66. Upon information and belief, Maxim had and has actual notice of the '739 patent, Maxim has been and is aware of its infringement, and Maxim's infringement has been and continues to be willful.

67. Freescale has been damaged by Maxim's infringement of the '739 patent and will continue to be damaged in the future unless Maxim is permanently enjoined from infringing the '739 patent.

SIXTH CLAIM FOR RELIEF**Infringement of the '798 Patent**

68. Freescale repeats and re-alleges paragraphs 30 through 42 as if fully set forth herein.

69. Maxim has been and is now directly infringing, and indirectly infringing by way of inducing infringement and/or contributing to the infringement, on Freescale's '798 patent in

1 this District and elsewhere by, making, using, offering for sale, selling, or importing products
2 and/or processes covered by at least one claim of the '798 patent, all to the injury of Freescale.

3 70. At relevant times, Freescale provided actual notice of the '798 patent to Maxim in
4 accordance with 35 U.S.C. § 287.

5
6 71. Upon information and belief, Maxim had and has actual notice of the '798 patent,
7 Maxim has been and is aware of its infringement, and Maxim's infringement has been and
8 continues to be willful.

9
10 72. Freescale has been damaged by Maxim's infringement of the '798 patent and will
11 continue to be damaged in the future unless Maxim is permanently enjoined from infringing the
12 '798 patent.

13 **PRAYER FOR RELIEF**

14
15 WHEREFORE, Freescale prays that:

16 1. This Court enter judgment against Maxim, and deny all of Maxim's requests for
17 relief and damages;

18
19 2. A judgment in favor of Freescale that Maxim has infringed the counterclaimed
20 Freescale patents directly and indirectly by way of inducing infringement and/or contributing to
21 the infringement of the counterclaimed Freescale patents;

22
23 3. A permanent injunction, enjoining Maxim and its officers, directors, agents,
24 servants, employees, affiliates, divisions, branches, subsidiaries, and parents from infringing,
25 inducing the infringement of, or contributing to the infringement of the counterclaimed Freescale
26 patents;

1 4. A judgment and order requiring Maxim to pay Freescale's damages for the
2 infringement of the counterclaimed Freescale patents, together with interest (both pre- and post-
3 judgment), post verdict and judgment damages, and treble damages for willful infringement as
4 provided by 35 U.S.C. § 284;

5
6 5. A judgment and order requiring Maxim to pay the costs of this action (including
7 all disbursements) and attorneys fees as provided by 35 U.S.C. § 285; and

8 6. Such other and further relief as the Court deems just and equitable.
9

10 **DEMAND FOR JURY TRIAL**

11 Freescale demands a jury trial on all issues triable of right by jury.
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Dated: May 2, 2008.

Respectfully submitted,

McKool Smith, PC

By /s/ Robert M. Manley

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**ATTORNEYS FOR DEFENDANT
FREESCALE SEMICONDUCTOR, INC.**

CERTIFICATE OF SERVICE

I hereby certify that on May 2, 2008, pursuant to Local Rule 5-6, I caused to be electronically filed and transmitted to the Clerk's Office *Defendant Freescale Semiconductor, Inc.'s Answer To Amended Complaint For Declaratory Judgment and Counterclaims* using the Court's CM/ECF System for filing and transmittal of a Notice of Electronic Filing to the following CM/ECF registrants:

Alan H. Blankenheimer, alan.blankenheimer@hellerehrman.com

Jo Dale Carothers, jodale.carothers@hellerehrman.com

Laura E. Underwood-Muschamp, laura.muschamp@hellerehrman.com

May 2, 2008

/s/ Nancy J. Felix

Nancy J. Felix
Legal Administrative Assistant
McKool Smith, P.C.

McKool Smith
A PROFESSIONAL CORPORATION • ATTORNEYS
DALLAS, TEXAS

EXHIBIT A



US005089722A

United States Patent [19]

Amedeo

[11] Patent Number: 5,089,722

[45] Date of Patent: Feb. 18, 1992

[54] HIGH SPEED OUTPUT BUFFER CIRCUIT WITH OVERLAP CURRENT CONTROL

[75] Inventor: Robert J. Amedeo, Austin, Tex.

[73] Assignee: Motorola, Inc., Schaumburg, Ill.

[21] Appl. No.: 503,012

[22] Filed: Apr. 2, 1990

[51] Int. Cl.⁵ H03K 17/16; H03K 19/094; H03K 5/12; H03K 17/687

[52] U.S. Cl. 307/443; 307/451; 307/542; 307/475; 307/548; 307/558; 307/263

[58] Field of Search 307/270, 443, 542, 572, 307/448, 451, 452, 585, 552, 555, 558, 568, 592, 594, 597, 246, 263, 242, 475, 547, 548

[56] References Cited

U.S. PATENT DOCUMENTS

4,772,812 9/1988 Desmarais 307/270 X
 4,820,942 4/1989 Chan 307/542
 4,885,485 12/1989 Leake et al. 307/542
 4,908,528 3/1990 Huang 307/542 X
 4,918,339 4/1990 Shigeo et al. 307/542

4,954,729 9/1990 Urai 307/263 X
 4,959,565 9/1990 Knecht et al. 307/542
 4,961,010 10/1990 Davis 307/542 X

Primary Examiner—Edward P. Westin

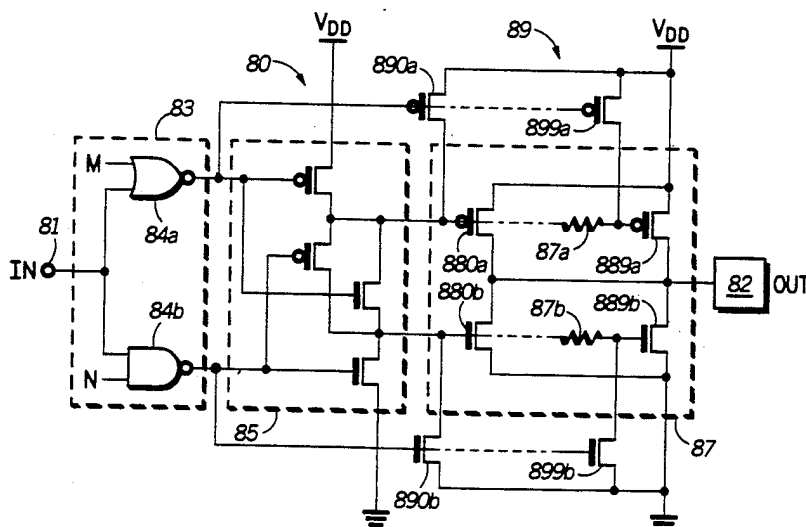
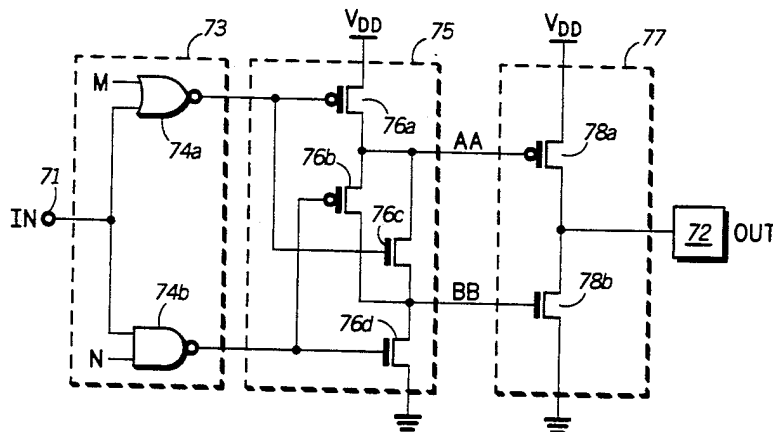
Assistant Examiner—David R. Bertelson

Attorney, Agent, or Firm—Robert L. King

[57] ABSTRACT

A pre-driver stage includes two pairs of series-stacked transistors for responding to input stage outputs and provides first and second outputs to an output driver stage. The first output becomes low at a certain delay period after the second output becomes low, and the second output becomes high at a certain delay period after the first output becomes high. Therefore, the turn-off of the active driver transistor is completed before the turn-on of the opposite output transistor, inhibiting an overlap current. In another form, the buffer circuit also uses assist transistors placed near the driver transistors for assisting the opposite driver transistors in turning off.

14 Claims, 4 Drawing Sheets



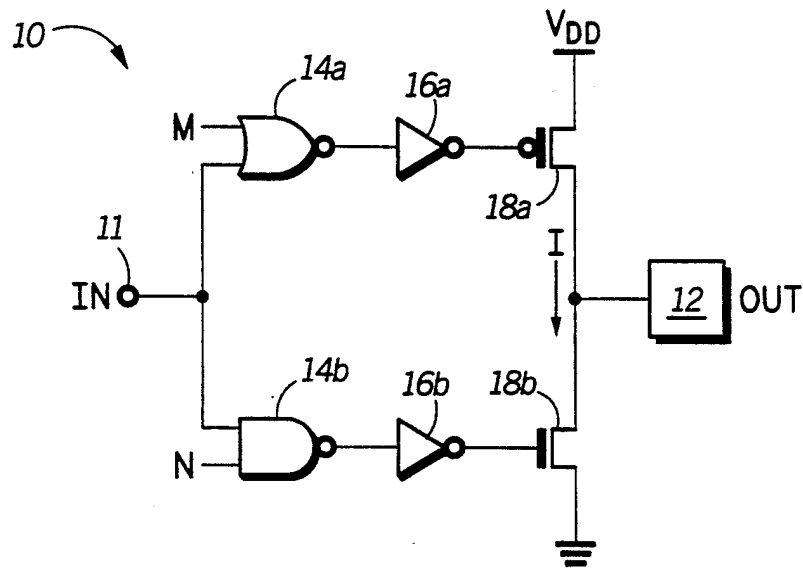


FIG. 1A
-PRIOR ART-

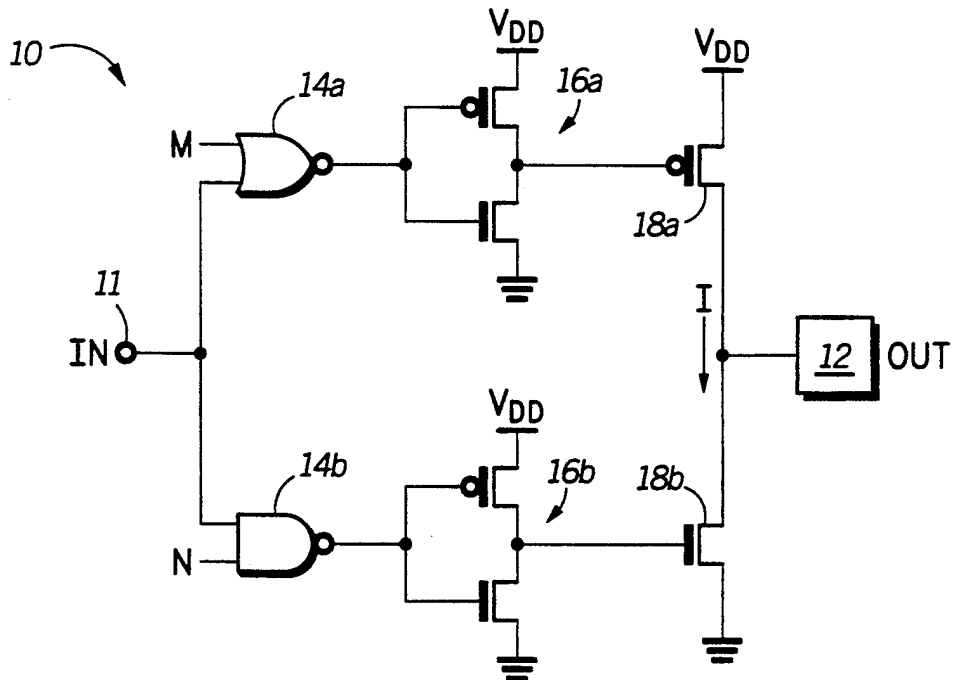
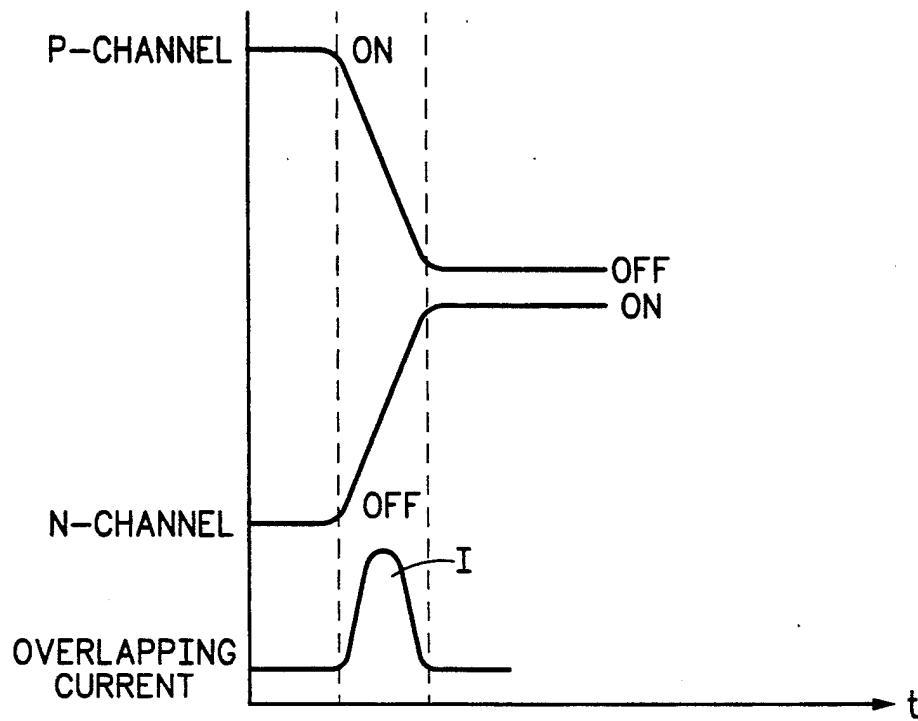
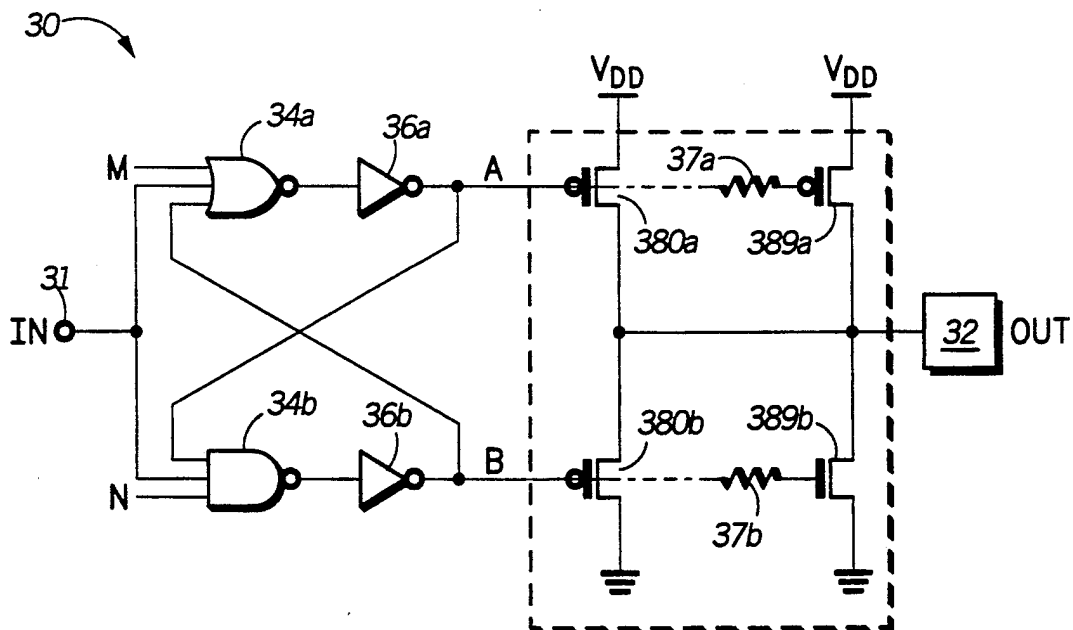


FIG. 1B
-PRIOR ART-

**FIG. 2****FIG. 3**
-PRIOR ART-

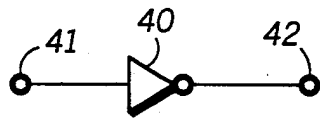


FIG. 4A

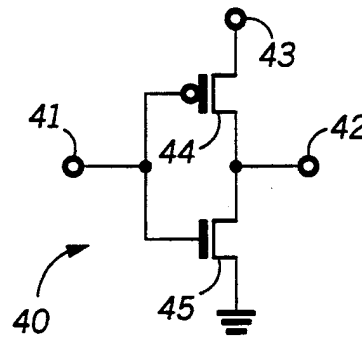


FIG. 4B

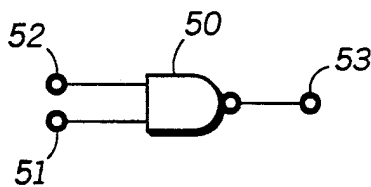


FIG. 5A

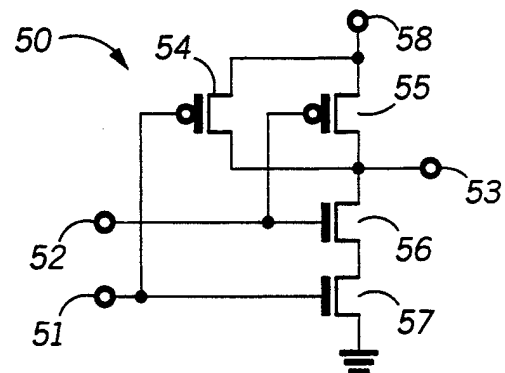


FIG. 5B

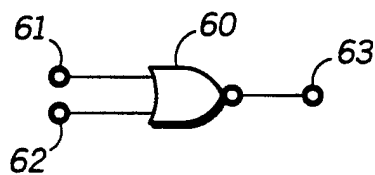


FIG. 6A

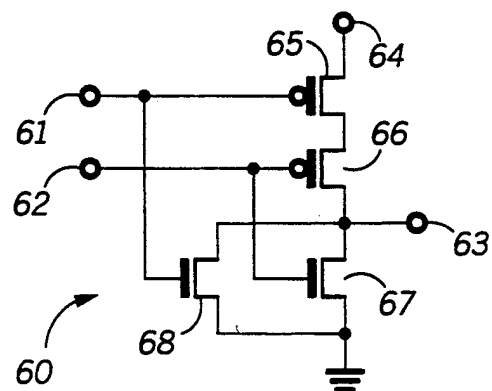
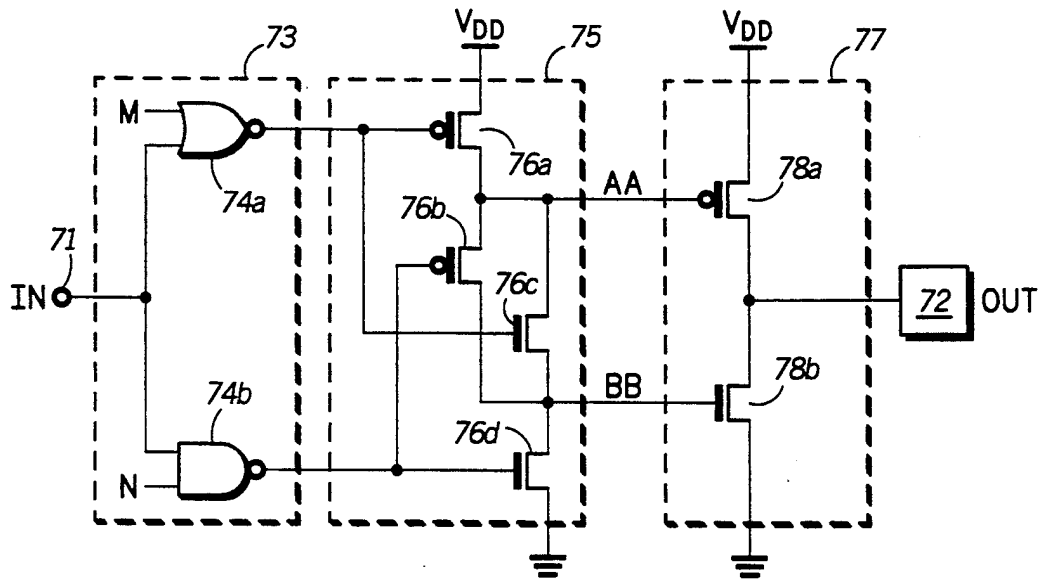
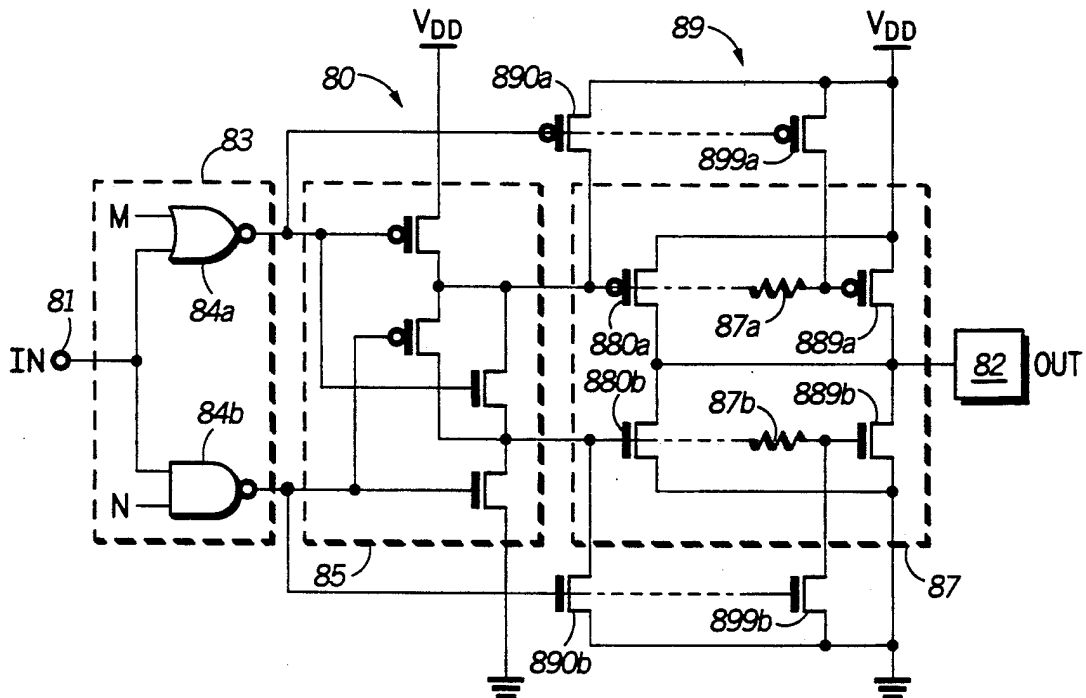


FIG. 6B

*FIG. 7**FIG. 8*

5,089,722

1

HIGH SPEED OUTPUT BUFFER CIRCUIT WITH OVERLAP CURRENT CONTROL

FIELD OF THE INVENTION

The present invention relates, in general, to an output buffer circuit. More particularly, the invention relates to a CMOS (complementary metal-oxide-silicon) output buffer circuit with high speed switching and large power handling capacity.

BACKGROUND OF THE INVENTION

Many digital output or driver circuits have been developed for use in MOS FET(field effect transistor) integrated circuitry, especially for use at output pads (terminals) of microprocessors or microcomputers. A CMOS output buffer having a complementary pair of transistors in an output stage is widely used and operates at a relatively high speed and reduces the internal power consumption when the buffer is in one or the other of its two logic states. However, the basic CMOS output buffer has a disadvantage that an overlapping current passes through the P-channel and N-channel transistor of the output stage in the buffer when it is switching from one logic state to the other.

In addition, it is desirable that the conventional buffer circuit be able to source (and sink) a large amount of current to (and from) external circuitry connected thereto. But, it is difficult to drive external large circuit loads by the conventional CMOS output buffer.

Attempts to overcome such defects of the single transistor pair CMOS output buffer include cross-coupling pre-drivers with input logic gates to provide propagation delays. Others have also connected multiple complementary transistor pairs in parallel in an output stage to increase the source and sink currents. However, such cross-coupling buffer circuits require additional interconnections which undesirably increase the complexity of the circuit, and the propagation delay period of the circuit cannot be controlled. Further, the multiple complementary transistor pair output buffer worsens the overlapping current problem, as described below in detail.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved output buffer circuit which has high switching speed with overlap current control.

More particularly, it is an object of the present invention to provide an improved output buffer circuit having large power driving capacity with overlap current control.

Yet another object of the present invention is to provide an improved output buffer circuit which can be easily implemented into existing circuits without additional process steps or area.

In carrying out the above and other objects of the invention there is provided, in one form, an output buffer circuit having a data input terminal for receiving a data signal, and an output signal terminal for providing an output signal. The output buffer circuit comprises an input stage, a pre-driver stage, and an output driver stage having a pair of driver transistors connected in series. The pre-driver stage includes two pairs of stacked transistors for responding to the input stage outputs and provides first and second outputs to the output driver stage. The first output assumes a first logic state after a first predetermined controlled delay

2

period after the second output assumes the first logic state, and the second output assumes a second logic state after a second predetermined controlled delay period after the first output assumes the second logic state. The turn-off of an active driver transistor in the driver stage is completed before the turn-on of a second driver transistor in the driver stage, thereby preventing an overlap current.

According to another feature of the invention, the output buffer circuit further comprises assist semiconductor devices placed near the corresponding driver transistors for assisting the driver transistors in turning off.

These and other objects, features, and advantages, will be more clearly understood from the detailed description below together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a partial schematic diagram of a known output buffer circuit having a basic CMOS driver;

FIG. 1B shows the circuit of FIG. 1A, illustrating the inverters schematically;

FIG. 2 is a graph illustrating the generation of an overlap current in an output driver;

FIG. 3 is a partial schematic diagram of another known output buffer circuit having a cross-coupling structure;

FIGS. 4A and 4B show, respectively, the symbol of an inverter and its schematic diagram when implemented utilizing MOS transistors;

FIGS. 5A and 5B show, respectively, the symbol for a NAND gate and its schematic diagram utilizing MOS transistors;

FIGS. 6A and 6B show, respectively, the symbol for a NOR gate and its schematic diagram utilizing MOS transistors;

FIG. 7 is a schematic diagram of one embodiment of an output buffer circuit of this invention; and

FIG. 8 is a schematic diagram of another embodiment of an output buffer circuit of this invention.

DETAILED DESCRIPTION OF THE INVENTION

As mentioned before, although a conventional basic CMOS output buffer has the advantage of low quiescent current, it also has a disadvantage of an overlap current when switching between logic states. First, a brief reference will be made to a basic CMOS output buffer.

FIG. 1A schematically shows an example of a known CMOS output buffer. As shown in FIG. 1A, a basic output buffer circuit 10 includes a data input terminal 11 for receiving a data logic signal IN, and an output signal terminal 12 for providing an output logic signal OUT to external circuitry (not shown). When buffer 10 is receiving a logically high signal at terminal 11, the logic high signal is applied to a first input of a NOR gate 14a, thereby causing NOR gate 14a to provide a logic low signal on its output lead which is connected to the input of an inverter 16a. The logic state of an enable signal M connected to a second input of NOR gate 14a is assumed to be a logic low. Inverter 16a supplies at an output a logic high output signal which is applied to the gate of a P-channel MOS (metal-oxide-silicon) FET (field effect transistor) 18a, thus making P-channel transistor 18a nonconductive.

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Simultaneously, the logic high signal at input terminal 11 is applied also to a first input of a NAND gate 14b with a second input receiving a logic high enable signal N, thereby causing NAND gate 14b to provide a logic low signal at its output which is connected to the input of an inverter 16b. Inverter 16b supplies on its output a logic high output signal which is applied to the gate of an N-channel MOS transistor 18b, thus making N-channel transistor 18b conductive.

In this way, with buffer 10 receiving a logic high data signal, P-channel transistor 18a is off (nonconductive) and N-channel transistor 18b is on (conductive), thus effectively connecting output signal terminal 12 to ground through N-channel transistor 18b and disconnecting output signal terminal 12 from the positive supply voltage V_{DD} . Therefore, a logic low output signal is provided and buffer 10 is allowed to sink current from external circuitry (not shown) connected to terminal 12.

Conversely, when buffer 10 is receiving a logic low input signal, the logic low input signal is applied to the first input of NOR gate 14a with the second input thereof receiving a logic low enable signal M, thereby causing NOR gate 14a to provide a logic high signal at its output which is connected to the input of inverter 16a. Inverter 16a supplies at its output a logic low output signal which in turn is applied to the gate of P-channel transistor 18a, thus making P-channel transistor 18a conductive.

Simultaneously, the logic low signal at input terminal 11 is applied also to the first input of NAND gate 14b with the second input thereof still receiving a logic high enable signal N, thereby causing NAND gate 14b to provide a logic high at its output which is connected to the input of inverter 16b. Inverter 16b supplies at its output logic low output signal which in turn is applied to the gate of N-channel transistor 18b, thus making N-channel transistor 18b nonconductive.

In this manner, with buffer 10 receiving a logic low data signal, output signal terminal 12 is effectively connected to positive supply voltage V_{DD} and is disconnected from ground, therefore providing a logic high output signal and allowing buffer 10 to source current to external circuitry (not shown).

However, in this basic CMOS output buffer 10, because each signal from inverters 16a and 16b respectively arrives at the gates of transistors 18a and 18b simultaneously, P-channel transistor 18a turns off and N-channel transistor 18b turns on at the same time, as shown by a graph in FIG. 2, and vice versa. That is, the period of transient logic state of transistor 18a overlaps with the transient period of transistor 18b. Therefore, during the transient periods of transistors 18a and 18b, a current I passes from supply voltage V_{DD} through transistors 18a and 18b to ground. This overlap current (sometimes called "spike current") is especially high in a large output buffer having high power driving capability. The overlap current I is undesirable because it increases internal current consumption and causes RFI (radio frequency interference) which adversely affects other circuitry.

FIG. 3 shows another example of another known output buffer designed to solve the overlap current problem. As shown in FIG. 3, a cross-coupled output buffer circuit 30 includes a data input terminal 31 for receiving a digital data input signal IN, and an output signal terminal 32 for providing an output signal OUT to external circuitry (not shown). Output buffer 30 also includes a predetermined number of pairs of P-and N-

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channel MOS transistors 380a, b through 389a, b as noted by the dashed lines. Input terminal 31 is connected to a first input of a NOR gate 34a and to a first input of a NAND gate 34b. The output of each of NOR gate 34a and NAND gate 34b is connected to an input of inverters 36a and 36b, respectively. Output signals A and B from inverters 36a and 36b, respectively, are applied to the gates of multiple P-channel and N-channel transistors 380a through 389a and 380b through 389b, respectively. The circuit structure of cross-coupled buffer 30 is almost the same as that of CMOS buffer 10 shown in FIG. 1A, except that the output leads of inverters 36a and 36b are cross-coupled to other inputs of the NAND gate 34b and NOR gate 34a respectively, as shown in FIG. 3.

When buffer 30 is receiving a logic high data input signal, P-channel transistors 380-9a are off and N-channel transistors 380-9b are on, thus effectively connecting output signal terminal 32 to ground through N-channel transistors 380-9b and disconnecting output signal terminal 32 from a positive supply voltage V_{DD} . Therefore a logic low output signal is provided and buffer 30 is allowed to sink a large amount of current from external circuitry (not shown) connected to terminal 32.

Conversely, when buffer 30 is receiving a logic low data input signal, output signal terminal 32 is effectively connected to positive supply voltage V_{DD} and is disconnected from ground, therefore providing a logic high output signal and allowing buffer 10 to source a large amount of current to the external circuitry.

When the data input signal IN changes from one logic state to the other, the transient behaviors of output signals A and B respectively from inverters 36a, 36b are different from the outputs of inverters 16a and 16b of buffer 10 shown in FIG. 1A.

When the data input signal IN changes from logic high to logic low, the output of NAND gate 34b changes from low to high after one NAND gate delay. Then output signal B of inverter 36b changes from high to low after one inverter delay, and thereafter turns off each of N-channel transistors 380-9b. On the other hand, when data input signal IN changes from high to low, all inputs of NOR gate 34a do not change to low at once. A cross-coupled second input of NOR gate 34a which is provided with output signal B by inverter 36b slowly changes to low after one NAND gate and one inverter gate delay. After that, output signal A of inverter 36a changes to low after one NOR gate and one inverter gate delay, and then turns on P-channel transistors 380-9a. Therefore, the turn-on of P-channel transistor 380a is delayed after the turn-off of N-channel transistor 380b by one NOR gate and one inverter gate delay period, thereby inhibiting overlap current.

Conversely, when data input signal IN changes from low to high, the turn-on of N-channel transistor 380b is delayed after the turn-off of P-channel transistor 380a by one NAND gate and one inverter gate delay period, to inhibit overlap current.

However, this cross-coupled output buffer 30 also has disadvantages. The delay period resulting from the cross-coupling is too long due to plural transistor feedback gates (explained below in more detail), and cannot be accurately controlled.

In the case where multiple complementary transistor pairs 380-9a, b are employed, the last transistors 389a, b turn off much later, because parasitic impedance such as resistances 37a, b exist between the gate of the first transistor 380a, b and the gate of the last transistor 389a,

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b. The parasitic impedance typically results, in part, from the nature of the physical layout implementation of buffer 30 which is often required to comply with certain rules, in part, to control the conventional and well documented di/dt problem. Due to the delay of the turn-off of the last transistors 389a, b, electrical currents pass, for example, through P-channel transistor 389a and N-channel transistor 380b during the transient periods. Accordingly, in order to eliminate such cross-flowing overlap currents, more delay of the turn-on of the transistors is required and therefore more transistors are needed to accomplish the more delay. However these transistors are expensive and difficult to install, and their delay can not be adequately controlled.

Now, reference will be made to the inside structures of an inverter, a NAND gate and a NOR gate. An inverter, such as inverters 16a, b shown in FIG. 1A, is comprised of two MOS transistors as shown in FIGS. 4A and 4B. FIG. 4A shows the symbol for an inverter 40 having an input terminal 41 and an output terminal 42. FIG. 4B shows the MOS transistor implementation of the inverter 40. As shown in FIG. 4B, inverter 40, again having input terminal 41 and output terminal 42, is constructed by suitably connecting a P-channel MOS transistor 44 and an N-channel MOS transistor 45, with a terminal 43 being connected to a positive supply voltage. Thus, inverter 40 requires two MOS transistors. Therefore it should be understood that the circuit of FIG. 1B is equivalent to buffer circuit 10 shown in FIG. 1A.

Similarly, a three-input NAND gate, such as NAND gate 34b of FIG. 3, requires six MOS transistors. A two-input NAND gate requires four transistors. As shown in FIGS. 5A and 5B, NAND gate 50, having inputs 51 and 52 and an output 53, is constructed utilizing P-channel MOS transistors 54 and 55, and N-channel MOS transistors 56 and 57, with a terminal 58 being connected to a positive supply voltage. Furthermore, a three-input NOR gate, such as NOR gate 34a of FIG. 3, requires at a minimum four MOS transistors. As shown in FIGS. 6A and 6B, two-input NOR gate 60, having inputs 61 and 62 and an output 63, is constructed utilizing P-channel MOS transistors 65 and 66, and N-channel MOS transistors 67 and 68.

Accordingly it should be understood that the propagation delay of NOR gate 34a of FIG. 3 is equal to two transistor gate delays when its output changes low to high. And it also should be understood that the propagation delay of NAND gate 34b of FIG. 3 is equal to two transistor gate delays when its output changes high to low.

In FIG. 3, when data input signal IN changes high to low, the turn-on of P-channel transistor 380a is delayed after the turn-off of N-channel transistor 380b by three transistor gate delay periods, which is too long and uncontrollable. Conversely, when data input signal IN changes from low to high, the turn-on of N-channel transistor 380b is delayed after the turn-off of P-channel transistor 380a by three transistor gate delay periods, which is also too long and uncontrollable.

The output buffer circuit according to the present invention will now be described in detail with reference to preferred embodiments thereof, which are illustrated in FIGS. 7 and 8.

For convenience of explanation, certain transistor gates are specifically described as P-channel or N-channel. However, those of skill in the art will understand that these are merely for ease of explanation and not

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intended to be limiting, and that the present invention includes arrangements where the channel types are inverted and/or where other combinations of P- and N-channels and voltage polarities are used. As is well understood, the FET devices of the circuit as well as other circuit components and their interconnections as illustrated may be fabricated as an integrated circuit in a single body of semiconductor material.

As shown in FIG. 7, an output buffer circuit 70 includes a data input terminal 71 for receiving a data input signal IN, an output signal terminal 72 for providing an output signal OUT, an input stage 73, a pre-driver stage 75, and an output driver stage 77. Input stage 73 comprises a NOR gate 74a and a NAND gate 74b. One input lead of NOR gate 74a and one input lead of NAND gate 74b are connected in common to receive the data input signal IN from input terminal 71. Other input leads of both gates 74a, b are used for receiving control or enable signals (not shown).

Pre-driver stage 75 comprises a first stacked pair of P-channel MOS FETs 76a and 76b, and a second stacked pair of N-channel MOS FETs 76c and 76d. P-channel transistors 76a and 76b are serially connected between a supply voltage V_{DD} and a juncture of serially connected N-channel transistors 76c and 76d. N-channel Transistors 76c and 76d are serially connected between ground and a juncture of P-channel transistors 76a and 76b. The output of NOR gate 74a is connected to the gates of P-channel transistor 76a and N-channel transistor 76c. The output of NAND gate 74b is connected to the gate of P-channel transistor 76b and N-channel transistor 76d. A first output AA of pre-driver stage 75 is derived at a node between P-channel transistors 76a and 76b. A second output BB of pre-driver stage 75 is derived at a node between N-channel transistors 76c and 76d.

It should be noted that pre-driver stage 75 has the same number of transistors as buffer circuit 10 of FIGS. 1A and 1B. That is, implementation of pre-driver stage 75 can be accomplished by using the same number of transistors as in the known circuit but rewiring them as shown in FIG. 7.

Output driver stage 77 comprises a complementary pair of a P-channel MOS FET 78a and an N-channel MOS FET 78b. The MOS FETs 78a and 78b are connected in series between voltage supply V_{DD} and ground. The gate of P-channel MOS FET 78a receives output AA from pre-driver stage 75. The gate of N-channel MOS FET 78b receives output BB from pre-driver stage 75. The output signal OUT is derived at a juncture of MOS FETs 78a and 78b.

In operation, when data input signal IN at input terminal 71 changes from logic low to high, the logic high signal is applied to a first input of NOR gate 74a thereby causing NOR gate 74a to generate a logic low signal at its output which is connected to the gates of transistors 76a and 76c. An enable signal M is at a logic low. Thus, P-channel transistor 76a turns on (conductive) and N-channel transistor 76c turns off (nonconductive), thus changing output AA to high immediately. High output AA is applied to the gate of P-channel transistor 78a, thus causing P-channel transistor 78a to turn off.

Simultaneously, the logic high input signal IN is applied also to a first input of NAND gate 74b with the other input lead receiving a logic high enable signal N, thereby causing NAND gate 74b to provide a logic low signal at its output which is connected to the gates of transistors 76b and 76d. Thus, P-channel transistor 76b

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turns on and N-channel transistor 76d turns off. Output BB becomes high at a delay period after output AA becomes high. This is because two stacked transistors 76a and 76b must turn on thereby providing output BB as a logic high while transistor 76a must turn on for output AA to be a logic high.

Therefore, N-channel transistor 78b does not become conductive until P-channel transistor 78a is completely nonconductive, thereby inhibiting overlap current. This delay period is determined by the sizes, especially the width-to length ratios (W/L), of transistors 76a, 76b; therefore it can be controlled.

Conversely, when data input signal IN at input terminal 71 changes from a logic high to low, the logic low signal is applied to the first input of NAND gate 74b thereby causing NAND gate 74b to generate a logic high signal at its output which is connected to the gates of transistors 76b and 76d. Thus, N-channel transistor 76d turns on and P-channel transistor 76b turns off, thereby changing output BB immediately to a logic low. Logic low output BB is applied to the gate of N-channel transistor 78b, thus causing N-channel transistor 78b to turn off.

Simultaneously, the logically low input signal IN is applied also to the first input of NOR gate 74a with the second input receiving a low enable signal M, thereby causing NOR gate 74a to generate a logic high signal on its output which is connected to the gates of transistors 76a and 76c. Thus, P-channel transistor 76a turns off and N-channel transistor 76c turns on. Output AA becomes low at a delay period after output BB becomes low. This is because two stacked or series-connected transistors 76c and 76d must turn on to provide a low output AA while only one transistor 76d must turn on for a low output BB.

Therefore, P-channel transistor 78a does not become conductive until N-channel transistor 78b is completely shut off, thereby inhibiting the overlap current. This delay period is determined by the transistor sizes, especially the width-to length ratios (W/L), 76c, 76d; therefore the delay can be controlled. That is, the transient period of transistor 78a does not overlap with the transient period of transistor 78b. Thus output buffer circuit 70 provides no or significantly reduced overlap current and less noise by turning off the active output transistor before turning on the opposing output transistor. By controlling the width-to length ratios (W/L) of transistors in pre-driver stage 75, the delay period can be very easily controlled. This pre-driver structure can be easily retrofitted into existing output buffer designs.

FIG. 8 shows another embodiment according to the present invention. An output buffer circuit 80 includes a data input terminal 81 for receiving an input data signal IN, an output signal terminal 82 for providing an output signal OUT, an input stage 83, a pre-driver stage 85, and an output driver stage 87. The circuit structure of output buffer 80 of this embodiment is almost the same as that of the first embodiment buffer 70 shown in FIG. 7 except that output driver stage 87 includes a predetermined number of plural pairs of P-channel and N-channel MOS transistors 880a, b through 889a, b, as noted by the dashed lines. Output buffer 80 further comprises assist transistors 89.

In the illustrated form, assist transistors 89 include P-channel MOS FETs 890a through 899a, and N-channel MOS FETs 890b through 899b. P-channel transistor 899a, for example, is placed near the gate of corresponding P-channel transistor 889a to enhance the turn-off of

transistor 889a. Other assist transistors 890 through 899 are placed near the gates of corresponding transistors 880 through 889. The gate of P-channel transistor 899a is connected to an output of NOR gate 84a, its source is connected to a positive supply voltage V_{DD} , and its drain is connected to the gate of transistor 889a.

It should be apparent from the previous discussion that significant impedance such as parasitic resistance 87a exists between the gate of transistor 880a and transistor 889a. This impedance causes overlap currents by slowing down the turn-off of the opposite drivers, as described above with reference to FIG. 3. Assist transistor 899a compensates the slowing down of the turn-off of opposite transistor 889a caused by the impedance, and facilitates the quick turn-off of transistor 889a. Other assist transistors may be similarly connected and function similarly. Assist transistors 890a, b through 899a, b are responsible for the turn-off direction only.

In this way, the combination of the stacked pre-driver transistors and the assist devices provide a faster and quieter output buffer circuit relative to what is conventionally used in CMOS applications. The output buffer circuit according to the invention provides great reduction in overlap current, RFI noise and power consumption.

While the present invention has been shown and described with reference to particular embodiments thereof, various modifications and changes thereto will be apparent to those skilled in the art and are within the spirit and scope of the present invention.

I claim:

1. An output buffer circuit having a data input terminal for receiving a data signal, and an output signal terminal for providing an output signal, comprising:

an input stage for receiving the data signal from the data input terminal and for providing input stage outputs;

a pre-driver stage for receiving the input stage outputs and for providing first and second outputs in response to the input stage outputs, said first output becoming logically low after a first predetermined controlled delay period after said second output becomes logically low, and said second output becoming logically high after a second predetermined controlled delay period after said first output becomes logically high; and

an output driver stage for receiving said first and second outputs from the pre-driver stage and for providing the output signal to the output signal terminal, said output driver stage including at least one complementary pair of serially connected output transistor devices, and said output signal being derived at a node between said serially connected output transistor devices,

said first and second outputs of the pre-driver stage being supplied only to said output driver stage and not to said input stage.

2. An output buffer circuit according to claim 1 wherein said input stage comprises a first logic gate and a second logic gate each having at least one input and an output, said inputs of the first and second logic gates being connected together for receiving the data signal.

3. An output buffer circuit according to claim 1 wherein said pre-driver stage comprises:

a first pair of transistors being serially connected between a first supply voltage terminal and said second output of the pre-driver stage, a node be-

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tween said first pair of transistors being connected to said first output of the pre-driver stage; and a second pair of transistors being serially connected between said first output of the pre-driver stage and a second supply voltage terminal, a node between said second pair of transistors being connected to said second output of the pre-driver stage.

4. An output buffer circuit according to claim 3 wherein control electrodes of said first and second pairs of transistors are connected to the input stage outputs.

5. An output buffer circuit according to claim 4 wherein said first pair of transistors are MOS transistors of a first conductivity, and said second pair of transistors are MOS transistors of a second conductivity.

6. An output buffer circuit according to claim 5 wherein said first conductivity is a p-type conductivity, and said second conductivity is an n-conductivity.

7. An output buffer circuit according to claim 3 wherein:

said first predetermined controlled delay period is determined by width-to-length ratios (W/L) of said second pair of transistors; and

said second predetermined controlled delay period is determined by width-to-length ratios (W/L) of said first pair of transistors.

8. An output buffer circuit according to claim 1 wherein:

said at least one complementary pair of output transistor devices comprises a p-channel MOS transistor and an n-channel MOS transistor.

9. An output buffer circuit according to claim 8 wherein:

a source of said p-channel MOS transistor is connected to a first supply voltage terminal;

a gate of said p-channel MOS transistor receives said first output from the pre-driver stage;

drain electrodes of both of said p-channel and n-channel MOS transistors are connected together for providing the output signal;

a gate of said n-channel MOS transistor receives the second output from the pre-driver stage; and

a source of said n-channel transistor is connected to a second supply voltage terminal.

10. An output buffer circuit having a data input terminal for receiving a data signal, and an output signal terminal for providing an output signal, comprising:

an input stage for receiving the data signal from the data input terminal and for providing input stage outputs;

a pre-driver stage for receiving the input stage outputs and for providing first and second outputs in response to the input stage outputs, said first output becoming logically low at a first predetermined controlled delay period after said second output

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becomes logically low, and said second output becoming logically high at a second predetermined controlled delay period after said first output becomes logically high;

an output driver stage including a plurality of complementary pairs of serially connected p- and n-channel MOS transistors, said plurality of pairs being connected in parallel between first and second supply voltage terminals, control electrodes of said p-channel transistors receiving said first output from the pre-driver stage, control electrodes of said n-channel transistors receiving said second output from the pre-driver stage, and all nodes between said MOS transistors in said pairs being connected together for providing the output signal to the output signal terminal; and

assist means for receiving the input stage outputs and for assisting said MOS transistors in turning off, said first and second outputs of the pre-driver stage being supplied only to said output driver stage and not to said input stage.

11. An output buffer circuit according to claim 10 wherein:

said input stage comprises a first logic gate and a second logic gate each having at least one input and an output, said inputs of the first and second logic gates being connected in common for receiving the data signal.

12. An output buffer circuit according to claim 10 wherein said pre-driver stage comprises:

a first pair of transistors being serially connected between a first voltage supply and said second output of the pre-driver stage, a node between said first pair of transistors being connected to said first output of the pre-driver stage; and

a second pair of transistors being serially connected between said first output of the pre-driver stage and a second voltage supply, a node between said second pair of transistors being connected to said second output of the pre-driver stage.

13. An output buffer circuit according to claim 12 wherein:

said assist means further comprise MOS transistors having gates connected to the input stage outputs, said assist means supplying signals for turning off the MOS transistors in the output driver stage.

14. An output buffer circuit according to claim 12 wherein:

said first predetermined controlled delay period is determined by width-to-length ratios (W/L) of said second pair of transistors; and

said second predetermined controlled delay period is determined by width-to-length ratios (W/L) of said first pair of transistors.

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EXHIBIT B

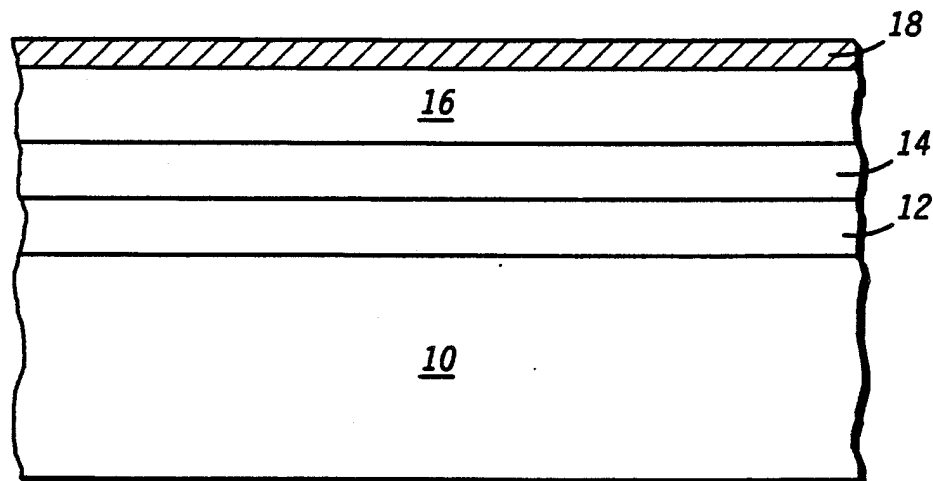
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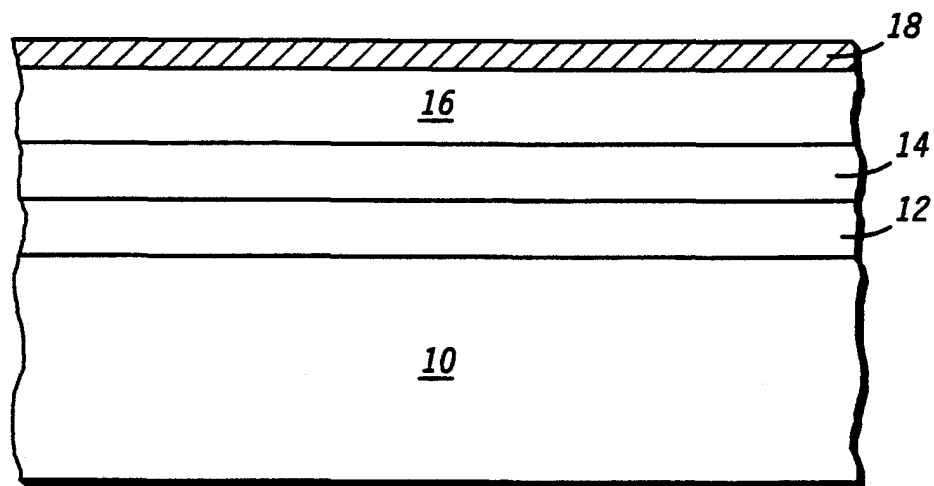
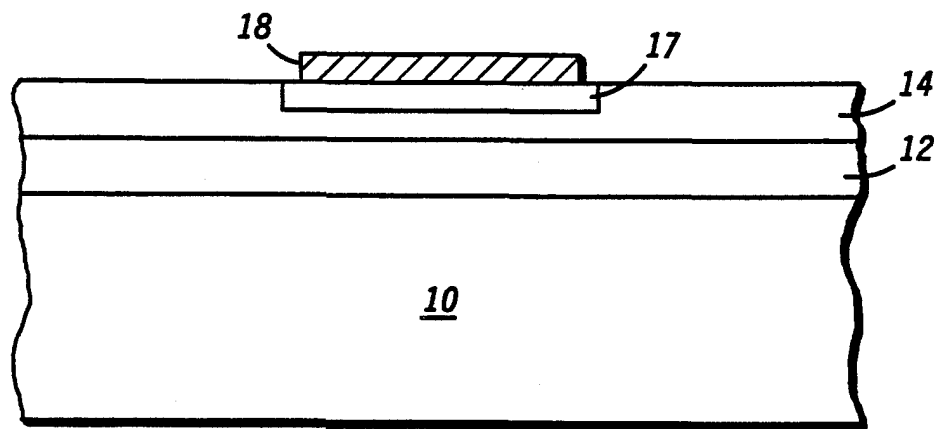
United States Patent [19][11] **Patent Number:** **5,105,250****Tam et al.**[45] **Date of Patent:** **Apr. 14, 1992**[54] **HETEROJUNCTION BIPOLAR
TRANSISTOR WITH A THIN SILICON
EMITTER**[75] **Inventors:** **Gordon Tam; Lynnita K. Knoch**, both
of Chandler, Ariz.[73] **Assignee:** **Motorola, Inc., Schaumburg, Ill.**[21] **Appl. No.:** **594,576**[22] **Filed:** **Oct. 9, 1990**[51] **Int. Cl.⁵** **H01L 29/72; H01L 29/161;**
H01L 29/04[52] **U.S. Cl.** **357/34; 357/35;**
357/16; 357/59[58] **Field of Search** **357/35, 34, 16, 59 H**[56] **References Cited****U.S. PATENT DOCUMENTS**

5,001,534 3/1991 Lunardi et al. 357/34

FOREIGN PATENT DOCUMENTS

8808206 10/1988 European Pat. Off. 357/34

OTHER PUBLICATIONS"Si/Si_{1-x}Ge_x Heterojunction Bipolar Transistors Pro-
duced by Limited Reaction Processing", by C. A. King
et al., published in IEEE, Electron Device Letters, vol.
10, No. 2, on Feb. 1989, pp. 52-54.*Primary Examiner*—Rolf Hille*Assistant Examiner*—Wael Fahmy*Attorney, Agent, or Firm*—Miriam Jackson; Joe E.
Barbee[57] **ABSTRACT**A heterojunction bipolar transistor having a thin,
lightly doped, silicon emitter disposed on a silicon-ger-
manium base layer exhibits low emitter resistance and
low emitter-base capacitance. The lightly doped silicon
emitter maintains the bandgap differential between sili-
con-germanium and silicon. The silicon emitter is fabri-
cated such that the silicon emitter will be substantially
depleted at zero bias, resulting in low emitter-base resis-
tance and emitter resistance.**10 Claims, 1 Drawing Sheet**

**FIG. 1****FIG. 2**

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HETEROJUNCTION BIPOLAR TRANSISTOR WITH A THIN SILICON EMITTER

BACKGROUND OF THE INVENTION

This invention relates, in general, to semiconductor devices, and more particularly, to a heterojunction bipolar transistor.

Heterojunction bipolar transistors exhibit electrical characteristics which are advantageous over the electrical characteristics of homojunction bipolar transistors. Silicon-germanium heterojunction bipolar transistor processing is compatible with existing silicon processing. Thus, silicon-germanium heterojunction bipolar transistors are preferred over other heterojunction bipolar transistors. In particular, silicon-germanium heterojunction bipolar transistors exhibit high emitter injection efficiency, reduced charge storage in the emitter, reduced or eliminated hole injection into the emitter. These characteristics are obtained because of the bandgap differential between the silicon and silicon-germanium metallurgical junction.

A silicon-germanium heterojunction bipolar transistor of the prior art consists of an N-type silicon collector, a P-type silicon-germanium base, and an N-type polysilicon layer. The N-type dopant from the polysilicon is diffused into the base to form an emitter region. The problem with this structure is that boron diffuses into the polysilicon layer or arsenic diffuses into the silicon-germanium base during the formation of the emitter. This diffusion degrades the bandgap differential by moving the metallurgical junction from the silicon-germanium and polysilicon interface into either the polysilicon layer or into the silicon-germanium base. Thus, the advantageous electrical characteristics described above are not exhibited.

A way of maintaining the metallurgical junction at the silicon-germanium and polysilicon interface is to prevent the diffusion of boron or arsenic from the respective layers. A structure in which the polysilicon layer is used as the emitter would solve this problem because the diffusion of boron or arsenic can be prevented. However, in this structure, the interface between the polysilicon layer and the silicon-germanium layer is poor, which results in the transistor exhibiting poor electrical characteristics, such as high leakage.

A transistor which solves this interface problem has been disclosed by King et al, in an article entitled, "Si/Si_{1-x}Ge_x Heterojunction Bipolar Transistors Produced by Limited Reaction Processing," published in IEEE Electron Device Letters, Vol. 10, No. 2, on Feb. 1989. The use of a thick silicon emitter of approximately 4,000 angstroms in thickness, instead of the polysilicon emitter eliminates the interface problem, and maintains the bandgap differential between the silicon-germanium layer and the silicon emitter layer in this case. However, in this structure, the thick silicon emitter must be lightly doped to avoid breakdown voltage problems and to avoid high emitter-base capacitance. A lightly doped, thick emitter exhibits high emitter resistance. Thus, it would be desirable to fabricate a heterojunction bipolar transistor in which the bandgap differential is ensured and also where emitter resistance and capacitance is low.

Accordingly, it is an object of the present invention is to provide an improved heterojunction bipolar transistor.

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Another object of the present invention is to provide a heterojunction bipolar transistor having low emitter-base capacitance and low emitter resistance.

A further object of the present invention to provide a heterojunction bipolar transistor in which the bandgap differential between silicon and silicon-germanium is maintained.

SUMMARY OF THE INVENTION

The above and other objects and advantages of the present invention are achieved by a heterojunction bipolar transistor having a thin, lightly doped, silicon emitter disposed on a silicon-germanium base layer. The lightly doped silicon emitter maintains the bandgap differential between silicon-germanium and silicon. The silicon emitter is fabricated such that it will be depleted at zero bias so that emitter-base capacitance and emitter resistance is low. In one embodiment, a polysilicon contact layer may be formed on the silicon emitter and can be heavily doped to further reduce emitter resistance. In a second embodiment, a thin ohmic contact region may be formed in the silicon emitter instead of the polysilicon contact layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates an enlarged, cross-sectional portion of a first embodiment of the present invention; and FIG. 2 illustrates an enlarged, cross-sectional portion of a second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates an enlarged, cross-sectional view of a portion of a heterojunction bipolar transistor in a first embodiment of the present invention. What is shown is a silicon layer 10 which acts as the collector of the heterojunction bipolar transistor, a silicon-germanium layer 12 which acts as the base, a thin silicon layer 14 formed on the silicon-germanium layer 12 which acts as the emitter, and a polysilicon layer 16 which acts as the emitter contact. A metal contact layer 18 is formed on polysilicon layer 16.

Silicon collector layer 10 is preferably doped N-type, using arsenic or antimony as a dopant. Silicon-germanium base layer 12 is preferably doped P-type, using boron as a dopant at approximately 1×10^{19} to 3×10^{19} atoms/cm³. The thickness of silicon-germanium base layer 12 is preferably approximately 500 angstroms. Thin silicon layer 14 is preferably lightly doped N-type, using arsenic as a dopant at approximately 8×10^{16} to 3×10^{17} atoms/cm³. The thickness of silicon layer 14 is preferably approximately 500 to 1500 angstroms. The thickness and doping of silicon layer 14 should be chosen such that silicon layer 14 will be substantially depleted at zero bias during normal operation. This is necessary in order to reduce emitter-base capacitance and emitter resistance. If silicon layer 14 is too thick, for example 4,000 angstroms as is described in the prior art, silicon layer 14 will not be depleted at zero bias and emitter resistance will be high. Polysilicon layer 16 is preferably heavily doped N-type using arsenic as a dopant.

After doping polysilicon layer 16, it is critical to anneal the heterojunction bipolar transistor by rapid thermal anneal to prevent degradation of the bandgap differential of silicon layer 14 and silicon-germanium layer 12 by preventing the diffusion of arsenic and boron from silicon-germanium layer 12 and silicon layer

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14. Polysilicon layer 16 is heavily doped in order to further lower emitter resistance. In a preferred embodiment, polysilicon layer 16 is doped using arsenic as a dopant at a level of approximately greater than 1×10^{19} atoms/cm³. The above layers are formed using techniques well known in the art. Note that only the active region of a heterojunction bipolar transistor is shown and described, however, this structure may be readily incorporated into many heterojunction bipolar process.

By including silicon layer 14 the metallurgical junction will be at the interface between silicon layer 14 and silicon-germanium layer 12. Thus, the advantage of the bandgap differential is not lost as in the prior art. In addition, the heterojunction bipolar transistor of the present invention has low emitter resistance and low emitter-base capacitance. The low emitter resistance is obtained by forming a heavily doped polysilicon layer 16. The low emitter-base capacitance is obtained by designing silicon layer 14 to be substantially depleted during operation. The heterojunction bipolar transistor of the present invention is thus a very high speed device that can be used for high speed digital and microwave applications.

FIG. 2 illustrates an enlarged, cross-sectional view of a portion of a heterojunction bipolar transistor in a second embodiment of the present invention. The same elements shown in FIG. 1 are referenced by the same numerals. FIG. 2 illustrates a structure similar to that of FIG. 1, however, in FIG. 2 polysilicon layer 16 is not utilized. In addition, silicon layer 14 is preferably slightly thicker than in FIG. 1. Silicon layer 14 is preferably approximately 1,000 to 2,500 angstroms so that a shallow emitter contact region 17 may be formed therein. Emitter contact region 17 is preferably formed by using a heavy dose of arsenic, and is just deep enough to provide ohmic contact to metal layer 18. In this second embodiment, as in the first embodiment, silicon emitter layer 14 is thin enough so that it is substantially depleted during operation. Thus, the structure of FIG. 2 also exhibits good electrical properties.

As can be readily seen, the heterojunction bipolar transistor of the present invention maintains the bandgap differential, thus exhibits high emitter injection efficiency, reduced charge storage in the emitter, reduced or eliminated hole injection into the emitter. In addition the heterojunction bipolar transistor of the present invention exhibits low emitter resistance and emitter-base capacitance by utilizing a thin silicon emitter layer.

We claim:

1. A heterojunction bipolar transistor, comprising:

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a collector;
a silicon-germanium base disposed on the collector;
a thin silicon emitter disposed on the silicon-germanium base, wherein a metallurgical junction is maintained at the silicon-germanium base and the thin silicon emitter interface; and
a polysilicon layer disposed on the thin silicon emitter.

2. The heterojunction bipolar transistor of claim 1 wherein the silicon emitter is of a thickness where the thin silicon emitter is substantially depleted at zero bias.

3. The heterojunction bipolar transistor of claim 2 wherein the silicon emitter is of a thickness of approximately 500 to 2,500 angstroms.

4. A heterojunction bipolar transistor comprising:
a collector;
a silicon-germanium base formed on the collector;
a thin silicon emitter formed on the silicon-germanium base, wherein the silicon emitter has a thickness and a doping level such that it is substantially depleted during normal operation, and wherein a metallurgical junction is maintained at the silicon-germanium base and the thin silicon emitter interface; and
a polysilicon layer formed on the silicon layer.

5. The heterojunction bipolar transistor of claim 4 wherein the silicon emitter is of a thickness of approximately 500 to 2,500 angstroms.

6. The heterojunction bipolar transistor of claim 4 wherein the polysilicon layer is heavily doped.

7. A heterojunction bipolar transistor, comprising:
an N-type collector;
a P-type silicon-germanium base formed on the collector;
an N-type, thin, lightly doped silicon emitter formed on the silicon-germanium base, wherein a metallurgical junction is maintained at the P-type silicon-germanium base and the N-type, thin, lightly doped silicon emitter interface; and
an N-type, heavily doped polysilicon layer formed on the silicon layer.

8. The heterojunction bipolar transistor of claim 7 wherein the thin, lightly doped silicon emitter is substantially depleted during normal operation.

9. The heterojunction bipolar transistor of claim 8 wherein the thin, lightly doped silicon emitter is doped at approximately 8×10^{16} to 3×10^{17} atoms/cm³.

10. The heterojunction bipolar transistor of claim 7 wherein the heavily doped polysilicon layer is doped at approximately 1×10^{19} atoms/cm³.

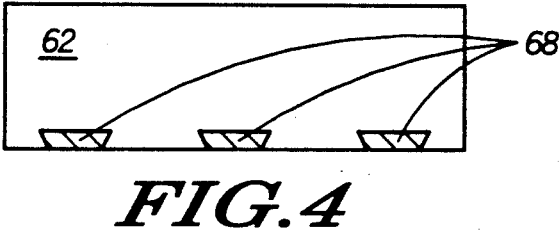
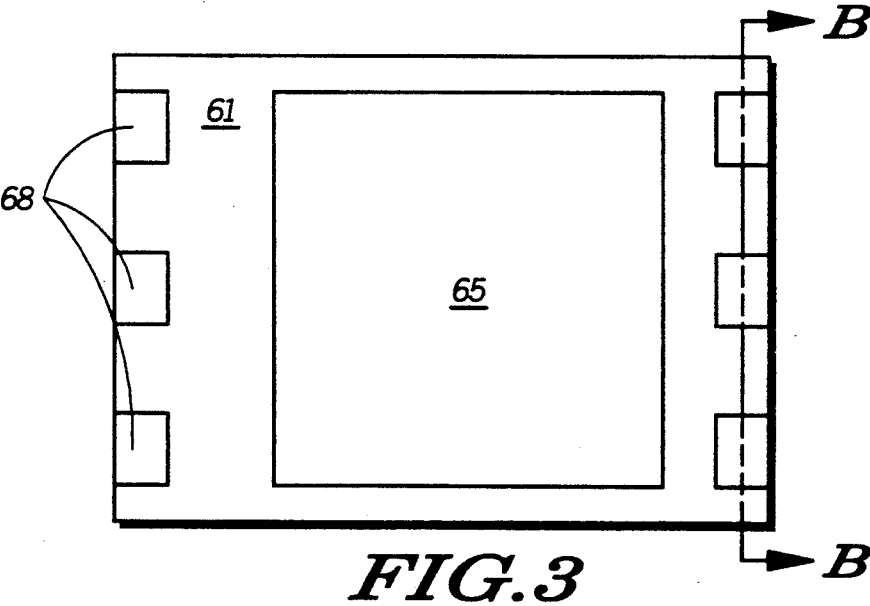
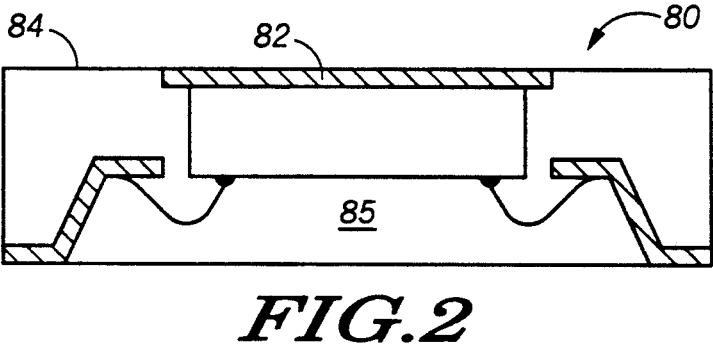
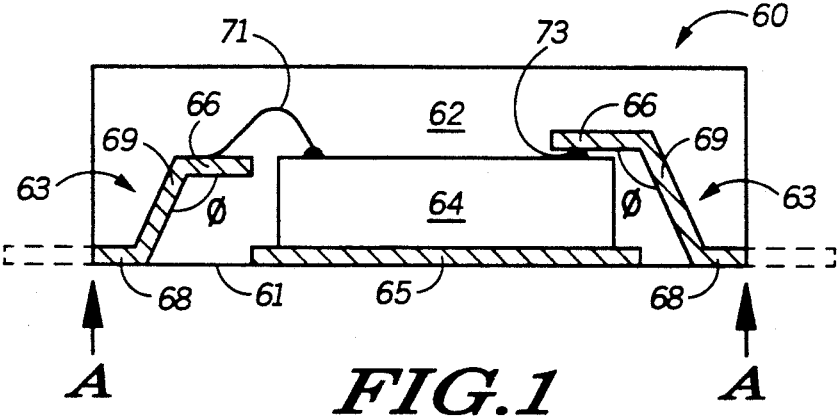
* * * * *

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EXHIBIT C



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LEADLESS SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME

This application is a continuation of prior application Ser. No. 07/651,165, filed Feb. 6, 1991, now abandoned.

CROSS-REFERENCE TO RELATED APPLICATION

This application is related to a commonly assigned co-pending patent application entitled, "SEMICONDUCTOR DEVICE HAVING DUAL ELECTRICAL CONTACT SITES AND METHOD FOR MAKING THE SAME," by McShane et al., Ser. No. 07/651,166, filed concurrently herewith.

TECHNICAL FIELD OF THE INVENTION

The present invention is related to semiconductor devices in general, and more specifically, to leadless semiconductor devices having thin package profiles and a method for making the same.

BACKGROUND OF THE INVENTION

In order to meet the demands of the growing electronics industry, semiconductor manufacturers are faced with many challenges in supplying suitable semiconductor devices. One challenge is to provide customers with very small, yet powerful, devices. However, this challenge is not easily met. Small devices are desirable because small devices require less mounting space on a substrate and have fewer problems with signal transmissions as compared to larger devices. At the same time, powerful devices are necessary in order to store and transmit a maximum amount of information. Yet as the power and performance of a device increases, the size of the device also increases. Much of this increase is due to a larger number of terminals, or leads, required to operate the device.

Keeping the size of a semiconductor device to a minimum is often achieved by using thin, fragile, densely spaced leads as electrical contacts to the device. However, the use of such leads creates a variety of manufacturing and handling problems. Handling devices with such fragile leads can result in bent and non-coplanar leads, making it difficult to properly mount the device to a substrate, such as a PC (printed circuit) board. Manufacturing devices with such closely spaced leads is itself difficult. Leadframes used in molded packages have a piece of metal, known as a dambar, to act as a dam for molding material. The dambar must be cut out from between the leads prior to using the device, usually by a punching operation. Closely spaced leads can be damaged by the punching operation. Furthermore, the small dimensions of a punching tool used for removing dambars from between fine leads make the punching tool susceptible to damage as well.

Although much of the effort devoted to reducing package size has concentrated on reducing the package width and length, it is also desirable for semiconductor devices to be thin, especially in consumer electronics applications. Therefore, a need exists for an improved semiconductor device, and more specifically for an improved semiconductor device which is leadless and has a thin package profile.

BRIEF SUMMARY OF THE INVENTION

The previously mentioned needs are fulfilled, and other advantages are achieved with the present inven-

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tion. In one form, a semiconductor device has a semiconductor device die. The semiconductor device die is electrically coupled to a plurality of conductive leads. Each lead has a first portion and a second portion, the first portion being separated from the second portion by an intermediate portion. A package body encapsulates the semiconductor device die and first and intermediate portions of the plurality of conductive leads. The second portions of the plurality of conductive leads are exposed on an edge and a bottom surface of the package body.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 illustrates, in cross-section, an embodiment of a semiconductor device in accordance with the present invention.

FIG. 2 illustrates, in cross-section, another embodiment of a semiconductor device in accordance with the present invention.

FIG. 3 illustrates, in planar view, the bottom surface of the semiconductor device of FIG. 1.

FIG. 4 illustrates, in cross-section, a view of the semiconductor device of FIG. 3 taken along the line B—B.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

The present invention has several advantages over conventional semiconductor devices. One advantage is that a semiconductor device in accordance with the present invention is externally leadless. Most known devices have leads which are external to a package body. The presence of external leads requires that a device occupy more space on a substrate, such as a printed circuit board, than if the device had no external leads. Furthermore, the presence of leads generates handling and manufacturing problems as discussed earlier. Some known semiconductor devices are considered to be leadless, for example a leadless chip carrier (LCC). However, most LCCs are formed from a multilayer ceramic material, and therefore LCCs are quite expensive. An overmolded device is also leadless, but overmolded devices require a semiconductor die to be mounted onto a PC board prior to encapsulation. Since an overmolded device contains a portion of a PC board, the cost of the device is significantly increased.

Another advantage of the present invention is that a semiconductor device can be made very thin, up to half the thickness of many conventional devices. Thin semiconductor devices are a competitive advantage in the consumer market for such applications as smart cards, cellular telephones, and pagers. Yet another advantage is that the present invention also allows a semiconductor device to have good heat dissipation, without increasing the size of the device. Heat dissipation is an important concern in high performance and high power consumption devices. Most methods of removing heat from a device, such as using heat sinks, increase the size of the device. The present invention can effectively dissipate heat without an increase in device size.

Illustrated in FIG. 1 is a semiconductor device in accordance with the present invention. Device 60 has a semiconductor device die 64 which is usually an integrated circuit. Also included in device 60 is a leadframe (not entirely shown) having a plurality of leads 63 and a die receiving area 65 also known as a die pad or flag. Conventional leadframe materials, such as copper, copper alloys, iron-nickel alloys, or TAB (tape automated bonding) leadframes, are suitable for use with the pres-

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ent invention. Semiconductor device die 64 is positioned at die receiving area 65, typically using an adhesive material, and is electrically coupled to the plurality of leads 63. The left portion of device 60 illustrated in FIG. 1 uses a wire bond 71 to couple a lead to the die, whereas the right portion of device 60 illustrates use of a TAB bond 73 or other type of lead-on-chip bond. Usually a semiconductor device contains only one type of coupling technique. The device of FIG. 1 has two different coupling techniques solely for illustrative purposes.

Device 60 is approximately one-half the thickness of a conventional molded semiconductor device. Most semiconductor devices have a package body which extends both above and below a plurality of leads of a leadframe. The device illustrated in FIG. 1 is thinner than many known devices because a protective package body 62 is formed only above the plurality of leads 63 of the leadframe. This is accomplished by forming the package in a one-sided mold tool or a mold tool having one planar platen. Typically, molded semiconductor device packages are formed in mold tools having an upper and a lower platen, each platen having a cavity. The platens are brought together such that the two cavities form a larger cavity which surrounds a semiconductor device die and inner portions of leads of a leadframe. An encapsulating material is introduced into the larger cavity to form a package body which completely surrounds a die and inner portions of the leads. The package body extends both above and below the die and the leads. Device 60, on the other hand, has package body 62 only formed above the leads 63 and semiconductor device die 64.

In accordance with the present invention, the leads 63 of device 60 in FIG. 1 have first portions 66, second portions 68, and intermediate portions 69. Second portions 68 of leads 63 are exposed on a bottom surface 61 of package body 62 and on the sides of the package body. Upon forming package body 62 about semiconductor device die 64, leads 63 will extend from the package body, as illustrated by the dashed lines in FIG. 1. The leads may then be formed into standard lead configurations, such as gull-wing, J-lead, through-hole, or the like. Preferably, leads 63 are severed at points A to create a leadless semiconductor device. Electrical contact to the semiconductor device is made through the second portions exposed on bottom surface 61 of the package.

As illustrated in FIG. 1, first portions 66 of leads 63 are portions of the leads which are electrically coupled to semiconductor device die 64. In the case of wire bond coupling, it is advantageous to have the bonding surface of a lead in the same plane as the bonding surface of the die. Naturally for the TAB bond illustrated, one surface must lie just above the other. Lead-on chip bonding may also be used in accordance with the present invention. Intermediate portions 69 of the leads are portions of the leads which join first portions 66 and second portions 68. In order to have the second portions of the leads exposed on the bottom surface of the package, yet have first portions coupled to the die, intermediate portions are at an angle with respect to both the first and second portions. For example, intermediate portions 69 of FIG. 1 are at an angle ϕ from first portions 66. Suitable angles for use with the present invention are substantially in the range of 90°-150°, although other obtuse angles could be used.

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FIG. 1 also illustrates that die receiving area 65 is exposed on the bottom surface 61 of package body 62. Having the die receiving area, also referred to as a flag, exposed on a surface of the package improves the thermal performance of the device. Heat is conducted from semiconductor device die 64 through die receiving area 65 to the ambient, thereby reducing the temperature of the device.

To further enhance thermal performance, a die receiving area could be exposed on the top surface of the package body. Because the bottom surface of the package is adjacent to a substrate, such as a PC board, heat dissipation can be improved by removing heat through the top surface of the package rather than through the bottom surface. A semiconductor device 80, illustrated in FIG. 2, in accordance with the present invention, has a die receiving area 82 exposed on a top surface 84 of a package body 85. Device 80 has a thin package profile similar to the device illustrated in FIG. 1, yet has the added benefit of allowing heat to dissipate from a top surface which will be more exposed to the ambient.

A semiconductor device in accordance with the present invention, such as device 60 of FIG. 1, can be mounted to a substrate, such as a printed circuit board, like other leadless devices. For example, a PC board is screen printed with a solder paste in a pattern which corresponds to the pattern of the exposed second portions of the leads. The device is then appropriately positioned on the PC board and the solder is reflowed. For more reliable board mounting, the exposed portions of the leads of the device can be pretinned or solder plated prior to mounting the device. This improves the wettability of the exposed portions of the leads and provides better coupling to the screen printed solder on the substrate. An alternative method of mounting a device in accordance with the present invention is with the use of solder balls. Solder balls could be attached to the exposed portions of the leads and then coupled to a substrate at a later point.

Illustrated in FIG. 3 is a bottom perspective of the semiconductor device illustrated in FIG. 1. Die receiving area 65 is exposed on bottom surface 61 of the package body. Also exposed on bottom surface 61 are second portions 68 of the leads. Second portions 68 are used to electrically access the semiconductor die (not shown) and are usually electrically coupled to a substrate, for example, by solder, solder balls, gold bumps, or the like. A cross-section of second portions 68 taken along the line B-B of FIG. 3 is illustrated in FIG. 4. The cross-sectional shape of second portions 68 is illustrated as being trapezoidal. While a trapezoidal shape is not an essential aspect of the present invention, it may be helpful to have a lead shape which secures or locks the leads into place in package body 62. Because more of the lead is exposed on the surface of the package than in conventional semiconductor devices, added features to keep leads in place may be necessary.

Thus it is apparent that there has been provided, in accordance with the invention, a leadless semiconductor device and a method for making the same that fully meets the advantages set forth previously. Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that modifications and variations can be made without departing from the spirit of the invention. For example, use of the invention is not limited to use in packages

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having one semiconductor die, but may also be used with multiple component semiconductor devices. Nor is it necessary that a device in accordance with the invention have an exposed die receiving area. Furthermore, the invention is not limited to using the electrical coupling methods described or illustrated. Likewise, any method of mounting a semiconductor device having a structure in accordance with the invention is suitable. It is not intended that the invention be limited to the substrate mounting techniques described. Therefore, it is intended that this invention encompass all such variations and modifications as fall within the scope of the appended claims.

I claim:

1. A leadless semiconductor device comprising:
 - a leadframe having a die receiving area and a plurality of leads extending outwardly from positions adjacent the die receiving area, each of the leads having first and second portions and an intermediate portion, the first portion of each lead being closer to the die receiving area than the second portion, and each of the first and second portions being separated by the intermediate portion thereof;
 - a semiconductor die positioned at the die receiving area of the leadframe and electrically coupled to the plurality of leads; and
 - a package body having a top surface, a bottom surface, and a perimeter, wherein the semiconductor die, the plurality of leads, and the die receiving area are completely contained within the package body and wherein a first surface of each of the second portions of the leads and an entire surface of the die receiving area are exposed on and substantially flush with one of either the top surface or bottom surface of the package body.
2. The semiconductor device of claim 1 wherein a second surface of each of the second portions of the leads is exposed on and substantially flush with the perimeter of the package body and wherein only the first and second surfaces of the leads are exposed.
3. The semiconductor device of claim 1 further comprising means for electrically coupling the second portions of the leads exposed on the bottom surface of the package body to a substrate.
4. The semiconductor device of claim 3 wherein the means for electrically coupling the second portions of the leads to a substrate comprises solder.
5. A leadless semiconductor device comprising:
 - a semiconductor die;
 - a plurality of conductive leads electrically coupled to the semiconductor die, each lead having a first portion for electrical connection to the die and a second portion for subsequent electrical connection to the device, the second portion being separated from the first portion by an intermediate portion; and
 - a molded package body completely containing the semiconductor die and the plurality of conductive leads wherein a first surface of each second portion is exposed on, and substantially flush with, a side of the package body and a second surface of each second portion is exposed on, and substantially flush with one of either a top surface or a bottom surface of the package body and wherein only the first and second surfaces of the leads are exposed.
6. The semiconductor device of claim 5 further comprising a die receiving area for receiving the semicon-

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ductor die and wherein a surface of the die receiving area is exposed on and flush with one of either a top surface of the package body or the bottom surface of the package body.

7. The semiconductor device of claim 5 wherein the first portions of the leads and the second portions of the leads are positioned in substantially parallel planes.

8. The semiconductor device of claim 5 wherein the first portion of each of the plurality of leads intersects the intermediate portion at an obtuse angle.

9. A method for fabricating a leadless semiconductor device comprising the steps of:

providing a semiconductor die;

providing a leadframe having a die receiving area and a plurality of leads extending outwardly from positions adjacent the die receiving area, each of the leads having first and second portions and an intermediate portion, the first portion being closer to the die receiving area than the second portion, and the first and second portions being separated by the intermediate portion;

electrically coupling each first portion of the plurality of leads to the semiconductor die;

encapsulating the semiconductor die and portions of the plurality of leads with a resin encapsulating material to form a package body which completely contains the first portions, intermediate portions, and second portions of the leads such that a first surface of each of the second portions of the leads and an entire surface of the die receiving area are exposed on, and substantially flush with, one of either a top surface or a bottom surface of the package body; and

severing the plurality leads to create a second surface of each of the second portions of the leads which is exposed on, and substantially flush with, a side of the package to form the leadless semiconductor device in which only the first and second surfaces of the leads are exposed.

10. The method of claim 9 further comprising the step of attaching the semiconductor device to a substrate by soldering the exposed second portions of the leads on the bottom of the package body to the substrate.

11. A method for fabricating a leadless semiconductor device comprising the steps of:

providing a semiconductor die;

providing a leadframe having a plurality of leads, each of the leads having first and second portions and an intermediate portion, the first portions of the leads being used for electrical connection to the die, the second portions of the leads being used for electrical connection to the device, and the first and second portions being separated by the intermediate portion;

electrically coupling the first portions of each of the plurality of leads to the semiconductor die;

forming a package body from a resin encapsulating material, the package body completely containing the semiconductor die and the first, second, and intermediate portions of the plurality of leads such that a first surface of each of the second portions of the leads is exposed on, and substantially flush with, either a top surface or a bottom surface of the package body, such that a second surface of each second portion of the leads is exposed on, and substantially flush with a side of the package body, and such that only the first and second surfaces of the leads are exposed; and

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plating the first and second exposed surfaces of the second portions of the leads with a conductive material.

with a conductive material comprises plating the exposed areas of the second portions of the leads with solder.

12. The method of claim 11 wherein the step of plating the exposed areas of the second portions of the leads 5

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,172,214

DATED : December 15, 1992

INVENTOR(S) : James J. Casto

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In claim 1, column 5, line 36:
after "package body" insert --wherein a second surface of each of the second portions of the leads is exposed on and substantially flush with the perimeter of the package body, and wherein only the first and second surfaces of the second portions of the leads are exposed--;

Cancel claim 2;

In claim 5, column 5, line 65:
after "second surfaces" insert --of the second portions--;

In claim 9, column 6, line 38:
after "second surfaces" insert --of the second portions--; and

In claim 11, column 6, line 67:
after "second surfaces" insert --of the second portions--.

On title page, "12 Claims, 1 Drawing Sheet" should read

--11 Claims, 1 Drawing Sheet--

Signed and Sealed this

Sixteenth Day of November, 1993



Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

EXHIBIT D



US005200362A

United States Patent [19][11] **Patent Number:** **5,200,362****Lin et al.**[45] **Date of Patent:** **Apr. 6, 1993**

[54] **METHOD OF ATTACHING CONDUCTIVE TRACES TO AN ENCAPSULATED SEMICONDUCTOR DIE USING A REMOVABLE TRANSFER FILM**

[75] **Inventors:** **Paul T. Lin; Michael B. McShane,**
both of Austin, Tex.; **Sugio Uchida;**
Takehi Sato, both of Nagano, Japan

[73] **Assignee:** **Motorola, Inc., Schaumburg, Ill.**

[21] **Appl. No.:** **756,952**

[22] **Filed:** **Sep. 9, 1991**

Related U.S. Application Data

[63] Continuation of Ser. No. 576,255, Aug. 31, 1990, abandoned.

Foreign Application Priority Data

Sep. 6, 1989 [JP] Japan 1-231323

[51] **Int. Cl.⁵** **H01L 21/56; H01L 21/58;**
H01L 21/60

[52] **U.S. Cl.** **437/207; 437/211**

[58] **Field of Search** **437/206, 211, 220, 207;**
264/272.17; 29/841, 855

[56] **References Cited****U.S. PATENT DOCUMENTS**

4,530,152 7/1985 Roch et al. 437/211
4,635,356 1/1987 Ohuchi et al. 437/211

FOREIGN PATENT DOCUMENTS

6292331 4/1987 Japan 437/211

Primary Examiner—Olik Chaudhuri

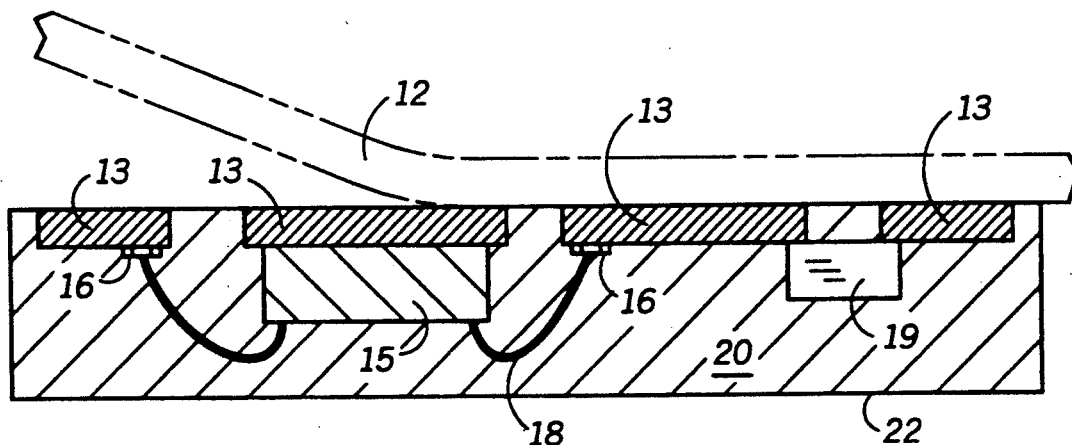
Assistant Examiner—David E. Graybill

Attorney, Agent, or Firm—Jasper W. Dockrey

[57] **ABSTRACT**

A semiconductor device and a method for its fabrication are disclosed. In a preferred embodiment, a pattern of conductive traces is formed on a film of transfer material. A semiconductor device die is interconnected to the pattern of conductive traces and a resin body is formed around the die, one side of the conductive traces, and the interconnecting means. The film of transfer material forms, at this stage of the process, one side of the package. The film of transfer material is then peeled from the pattern of conductive traces and the resin body to expose the other side of the pattern of conductive traces. Contact to the other side of the pattern provides electrical contact to the semiconductor device die.

8 Claims, 3 Drawing Sheets



U.S. Patent

Apr. 6, 1993

Sheet 1 of 3

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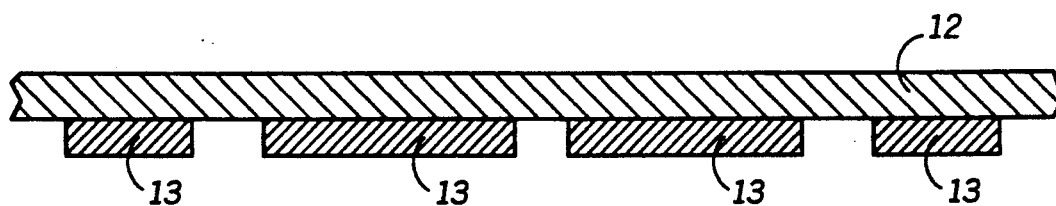


FIG. 1

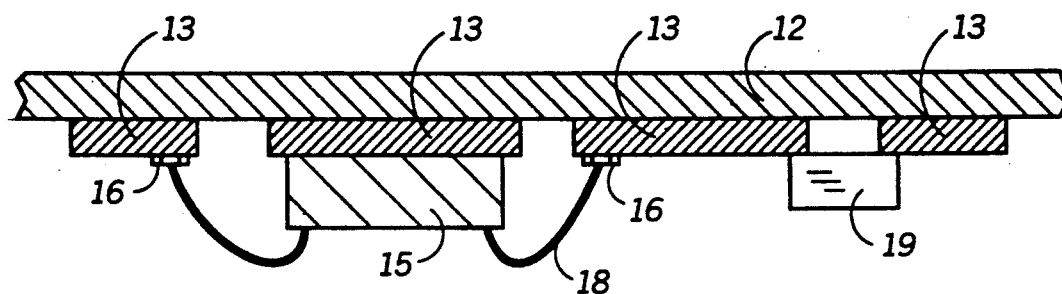


FIG. 2

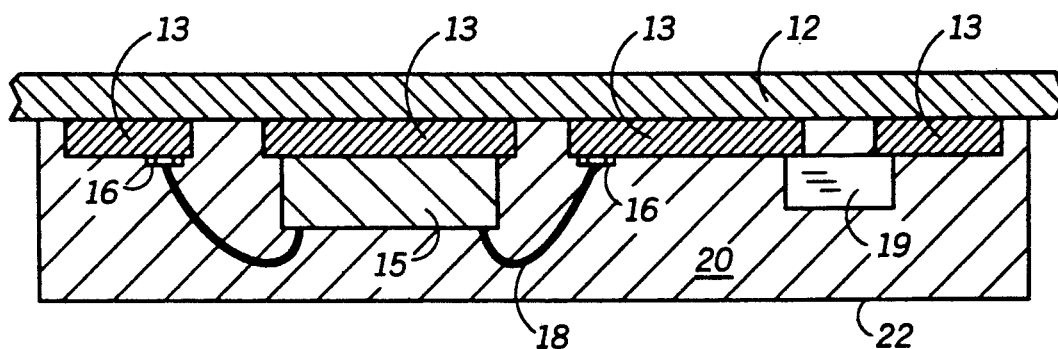


FIG. 3

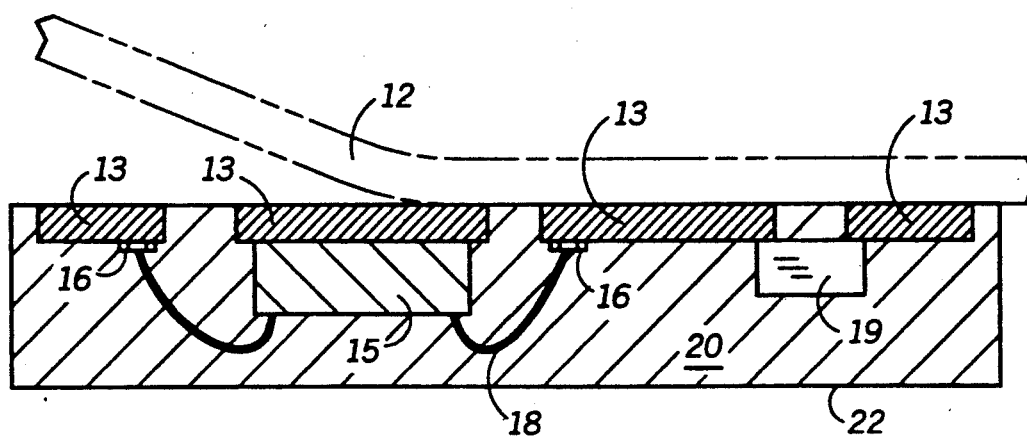


FIG. 4

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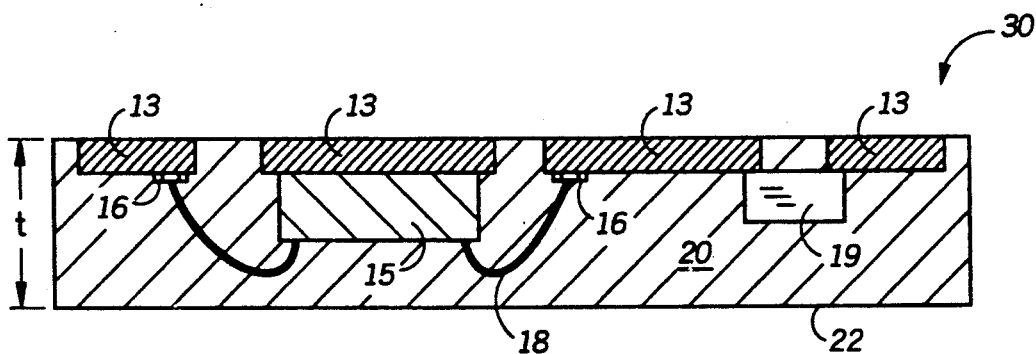


FIG. 5

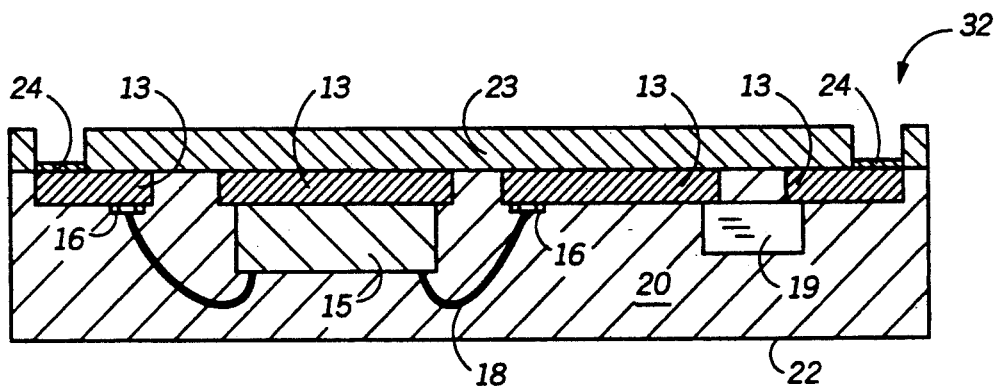


FIG. 6

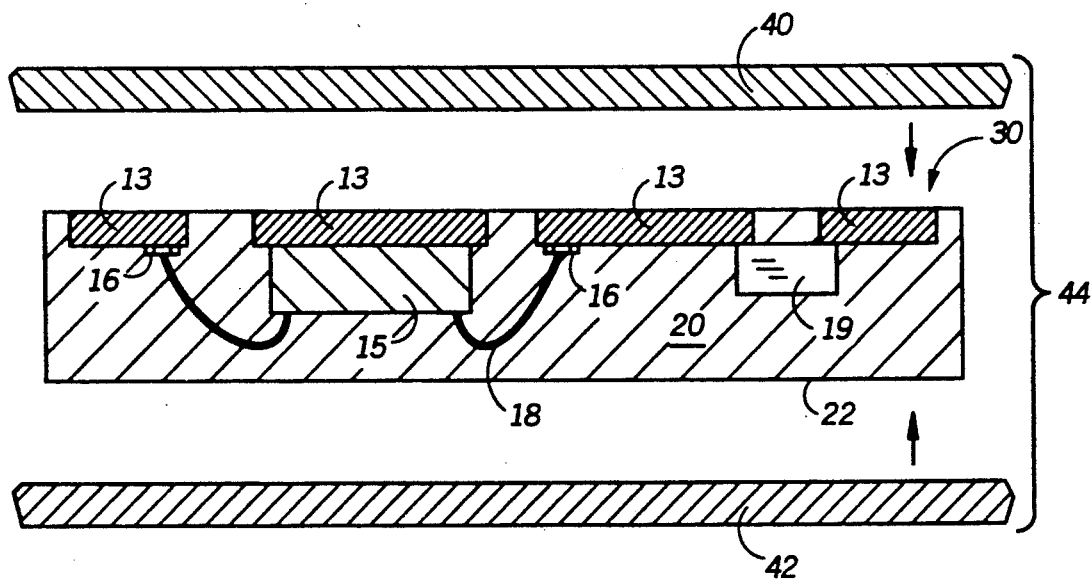


FIG. 7

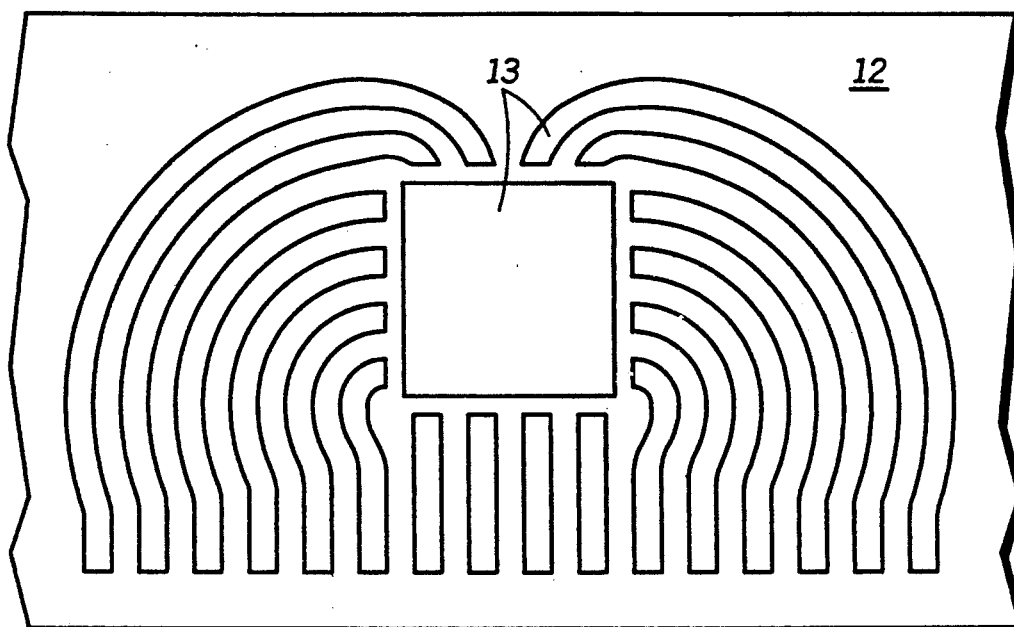


FIG. 8

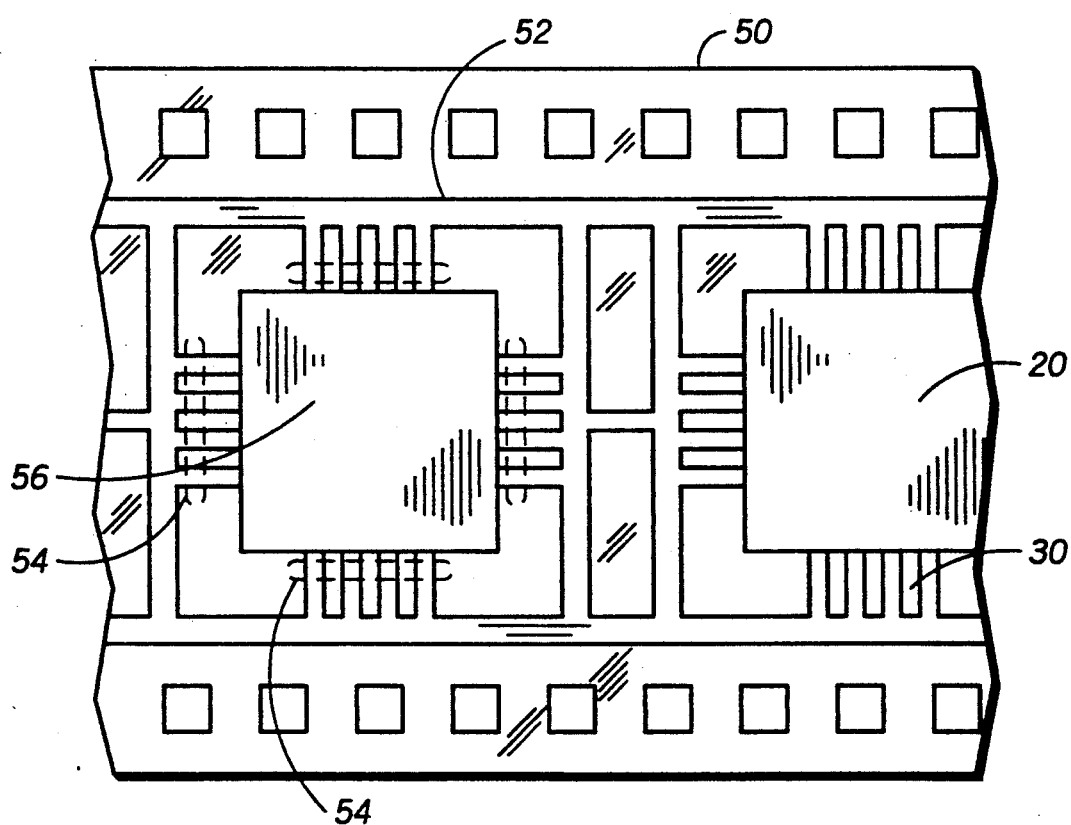


FIG. 9

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METHOD OF ATTACHING CONDUCTIVE TRACES TO AN ENCAPSULATED SEMICONDUCTOR DIE USING A REMOVABLE TRANSFER FILM

This is a continuation of application Ser. No. 07/576,255, filed Aug. 31, 1990, now abandoned.

BACKGROUND OF THE INVENTION

This invention relates to a resin encapsulated semiconductor device and to a method for its fabrication, and more specifically to a resin encapsulated semiconductor device capable of being fabricated in a thin format.

Semiconductor devices are widely used in various types of electronic products, consumer products, automobiles, integrated circuit cards, and the like. One feature of the semiconductor device which is important in many of these applications, and especially in such applications as the integrated circuit card, is the small size of the semiconductor device.

The semiconductor devices which are used in those various applications are usually packaged by either one of two methods. In one method, a semiconductor device die is placed in a package which is then individually mounted on a circuit substrate. In an alternate method, the semiconductor device die itself is mounted directly on the circuit substrate and then is usually provided with a protective encapsulation structure. The first mentioned method has the advantages that the device die is sealed in and protected by the package. The packaged device is easy to test, handle, and install and the encapsulating package provides the desired degree of protection against the environment. In contrast, the second described method in which the device die is connected directly to the substrate minimizes the area required by the die and thus allows a very high packing density. In this method, however, the device die is less easily handled and tested and is more subject to undesirable effects of the environment.

In selecting either of the above mentioned packaging techniques, it is necessary to compromise in the characteristics of the semiconductor device and the way it is utilized. In addition, either method requires that the semiconductor device be packaged on the interconnecting substrate such as a PC board, and thus has a problem of preventing the reduction in the thickness of the substrate so that the semiconductor device cannot be used in an application such as an IC card which requires an extremely thin substrate.

Thus a semiconductor device and a method for its fabrication were needed which would overcome the limitations of the foregoing semiconductor devices and methods.

BRIEF SUMMARY OF THE INVENTION

This invention provides a highly reliable packaged semiconductor device and a method for its fabrication which achieves a reduction in the thickness of the device without compromising the ease of handling a fully packaged device. In accordance with one embodiment of the invention, a semiconductor device is fabricated by providing a transfer film on which a pattern of conductive traces are provided. A semiconductor device die is interconnected to the pattern of conductive traces and a resin material is provided to encapsulate the semiconductor device die, one side of the pattern of conduc-

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tive traces, and the electrical interconnections between the traces and the die. The transfer film is then peeled from the encapsulated device and the pattern of conductive traces to expose the underside of the pattern of traces, at least a portion of which is available for making electrical contact to the semiconductor device die.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1-4 illustrate, in cross section, process steps in accordance with one embodiment of the invention for the fabrication of a semiconductor device;

FIGS. 5 and 6 illustrate, in cross section, semiconductor devices in accordance with two embodiments of the invention;

FIG. 7 illustrates schematically the fabrication of an integrated circuit (IC) card;

FIG. 8 illustrates a representative pattern of conductive traces on a transfer film; and FIG. 9 illustrates the fabrication of a plurality of semiconductor devices on an elongated transfer film in accordance with a further embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIGS. 1-4 illustrate, in cross section, process steps in accordance with one embodiment of the invention. As illustrated in FIG. 1, a transfer film 12 is provided with a pattern of conductive traces 13 on one side of the film. A representative and illustrative pattern of such traces is shown in FIG. 8. Transfer film 12 is a sheet film of flexible material such as "Kapton" or polyester upon which the pattern of conductive traces is formed.

The pattern of conductive traces can be formed in a number of different ways. In accordance with a preferred embodiment of the invention, a foil of conductive material such as copper is laminated to the transfer film 12 and is subsequently patterned using conventional photolithographic patterning and etching. Alternatively, the pattern of conductive traces can be formed, for example, by evaporating a layer of metal or other conductor onto the surface of the transfer film and then patterning that evaporated layer. If the evaporated layer is not of sufficient thickness to reduce the series resistance to a low enough value, the thickness can be increased by plating additional material onto the evaporated film. Still further, the pattern of conductive traces can be formed by first applying a reverse photoresist mask to the transfer film, evaporating a conductive material onto the photoresist and the transfer film, and then using a lift off process to remove the unwanted conductive material. In yet another embodiment, a pattern of traces is formed from a thin sheet of metal and that pattern of traces is then laminated to the transfer film.

A semiconductor device die 15 is electrically interconnected to the pattern of conductive traces. The interconnection is accomplished by wirebonds 18 or by other conventional means such as TAB tape, or the like. The semiconductor die can be affixed to a portion of the pattern of conductive traces, for example by solder, conductive epoxy, or the like or can be attached to the pattern only by the interconnecting means 18. If the die is attached to a portion of the pattern of conductive traces, that portion can be used, if necessary, as an electrical contact to a substrate of the semiconductor device die. As also illustrated in FIG. 2, additional circuit elements 19 can also be attached to and interconnected with the pattern of conductive traces. Circuit element

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19 can be, for example, a resistor, diode, capacitor, or the like. The additional circuit element, which can also be an additional semiconductor device die, can be connected between traces, as illustrated, or can be bonded to the conductive traces as is device die 15.

The portion 16 of the pattern of conductive traces to which the wirebonds or other interconnecting means are joined can be prepared especially to accommodate the attachment of the interconnecting means. For example, the bonding area 16 can be plated with gold, treated to smooth the area, or otherwise treated to enhance the reliability of the interconnection.

As illustrated in FIG. 3, the process continues by the encapsulation of the semiconductor device die 15, additional circuit element 19, interconnecting means 18, and one side of the pattern of conductive traces by an encapsulating resin 20 to form a protective body 22. Body 22 is formed in conventional manner, such as by transfer molding in which the transfer film 12 with the attached semiconductor device die 15 is inserted into a mold cavity and the encapsulating resin is forced into the cavity at a high temperature and high pressure. Alternatively, body 22 can be made by injection molding, pour molding, or in a "glop top" process. In each of these encapsulating operations, the resin material is formed on one side of transfer film 12; that is, the transfer film, at this stage of the process, forms one side of the package. The resin material thus surrounds the semiconductor device die, the interconnecting means, and one side of the pattern of conductive traces, plus any additional electronic components which are attached to the conductive traces.

Following the encapsulation operation, as illustrated in FIG. 4, the transfer film 12 is peeled or removed from the surface of the encapsulated device leaving a resin encapsulated device with one side of the conductive traces exposed and available to provide electrical contact to the semiconductor device die. In forming the pattern of conductive traces on transfer film 12, for example by applying a layer of electrolytic copper foil to the transfer film, it is especially advantageous if the surface of the foil which is to contact the transfer film is smooth and the opposite side is rough. The smooth surface facilitates the peeling away of the transfer film after the encapsulation operation and the rough surface enhances the adherence of the resin material to the pattern of conductive traces.

FIG. 5 illustrates, again in cross section, the completed semiconductor device 30 after the transfer film has been removed. Device 30 includes semiconductor device die 15 which is enclosed within an encapsulating resin body 22. Exposed on one side of the resin body are portions of one side of the pattern of conductive traces 13. These conductive traces can be directly contacted for making electrical contact to the semiconductor device die. No thick device "header" or leadframe is necessary for mounting the device die, and so the thickness "t" is minimized. In addition to making contact to the conductive traces for the purpose of making electrical contact, some of the traces, such as trace 13 upon which device die 15 is mounted, can be contacted by a heat sink (not shown) in order to conduct heat away from the die during operation.

FIG. 6 illustrates, in cross section, a semiconductor device 32 in accordance with an alternate embodiment of the invention. This embodiment is similar to device 30 illustrated in FIG. 5 except that a protective coating 23 is applied to the exposed surface of the pattern of

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conductive traces 13. The protective coating can be, for example, a low temperature deposited oxide, polyimide, adhesively applied insulating film, or the like. Openings 24 are formed through insulating film 23 to expose selected portions of the pattern of conductive traces. Gold plating or other metallic plating can be applied to the exposed portions of the conductive traces to protect against corrosion of the those exposed portions and also to enhance the ability to electrically contact those portions. In device 32 only the contacts 24 are exposed and the rest of the semiconductor device is encapsulated either by encapsulating body 22 or by the protective film 23.

FIG. 7 illustrates schematically, in exploded view, a further embodiment of the invention. As illustrated in FIG. 7, an IC card structure or the like is fabricated by laminating a device such as device 30 between upper 40 and lower 42 plastic sheets. The three components are laminated together to form an IC card device 44. The term "IC card" is used to describe the debit cards and the like which incorporate an integrated circuit to update the financial or other status of the card as money is deposited or as the card is used. IC device 30 provides the intelligence included within the IC card. The flat plastic sheets 40, 42 provide a useful card size and include identifying information embossed on the faces as well as other information and user interface. The underside of sheet 40 may include a pattern of traces which interface with the pattern of traces 13 on device 30. The traces may be coupled together with solder bumps, conductive epoxy, or the like, or merely by the pressure of the lamination itself. Electrical contacts on the edge of one of the plastic sheets then provides an external electrical access to the device 30. Alternatively, device 30 itself, with a pattern as that illustrated in FIG. 5, may directly provide the external contact. For example, sheet 40 may be provided with a window or windows (not shown) which expose the pattern of traces on device 30 so that contact, for example by a card reader machine, can be made directly to those traces.

FIG. 9 illustrates, in plan view, the fabrication of semiconductor devices in accordance with a further embodiment of the invention in which a plurality of devices can be fabricated simultaneously. An elongated transfer film 50 provides a plurality of groups of patterns of conductive traces (parts of two groups are illustrated) on one surface thereof. The conductive traces are interconnected by a bus line 52 which allows the plurality of traces to be electrolytically plated. The patterns of conductive traces can be made, for example, by evaporating a film of conductive material onto the surface of elongated transfer film 50, patterning that evaporated film into the desired pattern, and then electroplating to achieve the desired thickness of conductive material. A semiconductor device die is mounted and interconnected to each of the groups of conductive traces and the die, interconnections, and one side of the conductive traces are encapsulated within a resin body 56. After the resin encapsulation, which is carried out in a manner similar to that described above, the elongated transfer film is peeled off or otherwise removed to expose the reverse side of the conductive traces. Either before or after the transfer film is removed, the traces can be severed along the lines 54 to electrically disconnect the individual devices so that they can be tested.

Thus it is apparent that there has been provided, in accordance with the invention, a semiconductor device and method for its fabrication which overcomes the

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problems associated with the prior art devices and methods. Although the invention has been described and illustrated with reference to specific embodiments thereof, it is not intended that the invention be limited to these illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. For example, other patterns of conductive traces can be used and additional devices can be interconnected as needed. Additionally, other methods for forming both the conductive traces and for the encapsulation of the devices are possible. Thus it is intended to encompass within the invention all such variations and modifications as fall within the scope of the appended claims.

We claim:

1. A process for fabricating a semiconductor device comprising the steps of:
 providing a transfer film;
 providing a pattern of conductive traces on said transfer film;
 providing a semiconductor device die;
 forming electrical interconnections between said pattern of conductive traces and said semiconductor device die;
 providing a resin material on one side of said transfer film to encapsulate said semiconductor device die,

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said electrical interconnections, and a portion of said pattern of conductive traces; and
 removing said transfer film to expose one side of said pattern of conductive traces.

2. The process of claim 1 further comprising the step of forming a layer of insulating material over portions of said one side and leaving contact areas of said pattern exposed.

3. The process of claim 1 further comprising the step of laminating said semiconductor device die and said resin material between two sheets of plastic material.

4. The process of claim 3 wherein said step of laminating leaves exposed a portion of said one side.

5. The process of claim 4 further comprising the step of plating contact metal onto said exposed portion.

6. The process of claim 1 wherein said step of forming a pattern of conductive traces comprises the steps of:
 forming a continuous layer of conductive material on said transfer film; and
 selectively etching said continuous layer to form said pattern of conductive traces.

7. The process of claim 6 wherein said step of forming a continuous layer comprises laminating a layer of conductive foil to said transfer film.

8. The process of claim 6 wherein said step of forming a continuous layer comprises evaporating a layer of metal onto said transfer film.

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EXHIBIT E

US005434739A

United States Patent [19]

[11] Patent Number: 5,434,739

[45] **Date of Patent:** Jul. 18, 1995

[54] REVERSE BATTERY PROTECTION CIRCUIT

[75] Inventor: **Karl R. Heck, Phoenix, Ariz.**

[73] Assignee: **Motorola, Inc., Schaumburg, Ill.**

[21] Appl. No.: 75,839

[22] Filed: **Jun. 14, 1993**

[51] **Int. Cl.⁶** **H02H 3/18**

[52] U.S. Cl. 361/84; 361/56

[58] **Field of Search** 361/84, 85, 92, 90,
361/56, 91, 77

[56] References Cited

U.S. PATENT DOCUMENTS

5,126,911 6/1992 Contiero et al. 361/84

Primary Examiner—Marc S. Hoff

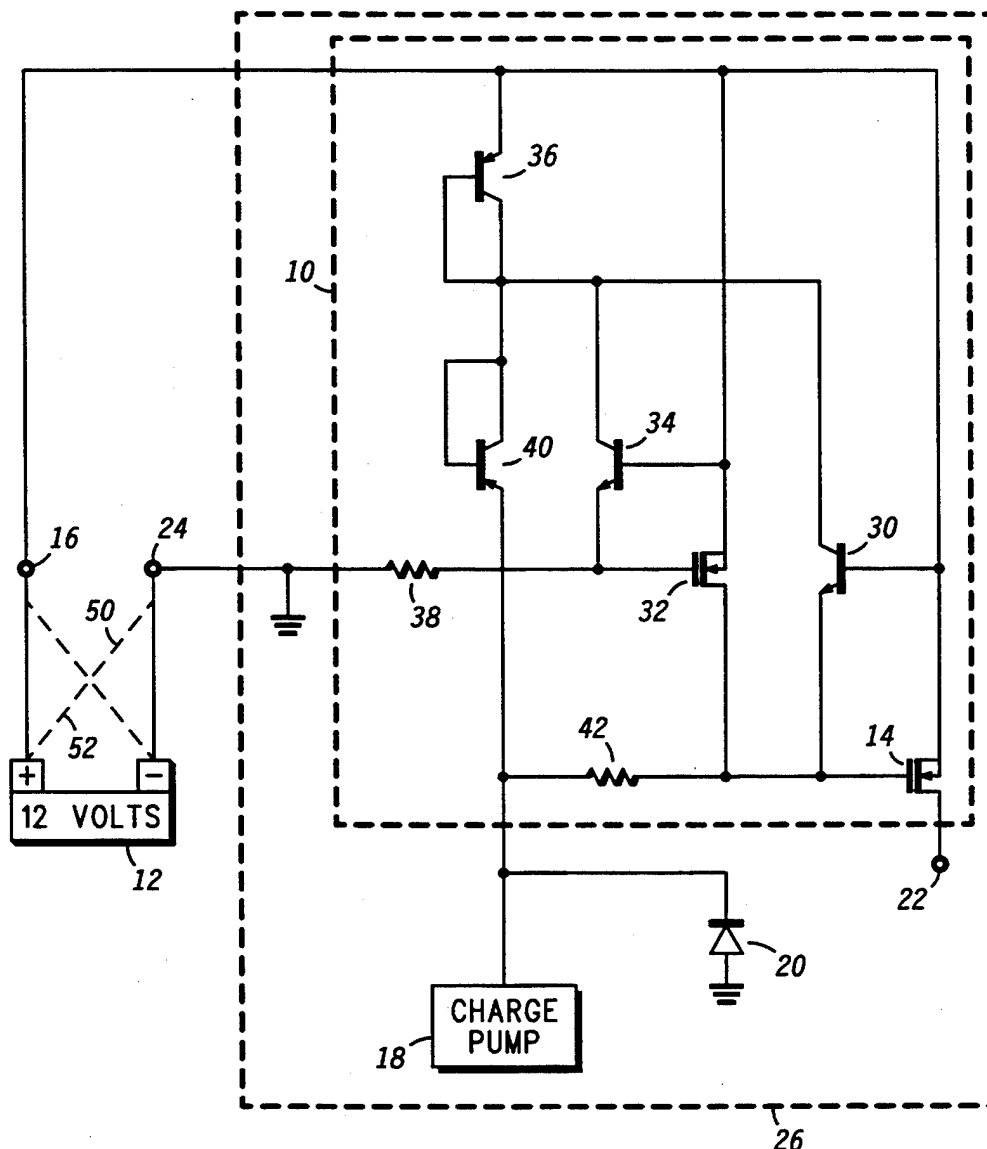
Assistant Examiner—S. Jackson

Attorney, Agent, or Firm—Rennie William Dover

[57] **ABSTRACT**

A protection circuit (10) for protecting internal circuitry of an integrated circuit (26) from a reverse battery connection has been provided. The protection circuit includes a pass transistor (14) which is rendered operative when the supply voltage is properly connected to the integrated circuit. However, when the power supply is improperly connected, a second transistor (32) becomes active thereby rendering the pass transistor inactive and not allowing the reverse supply voltage to be applied to the internal circuitry.

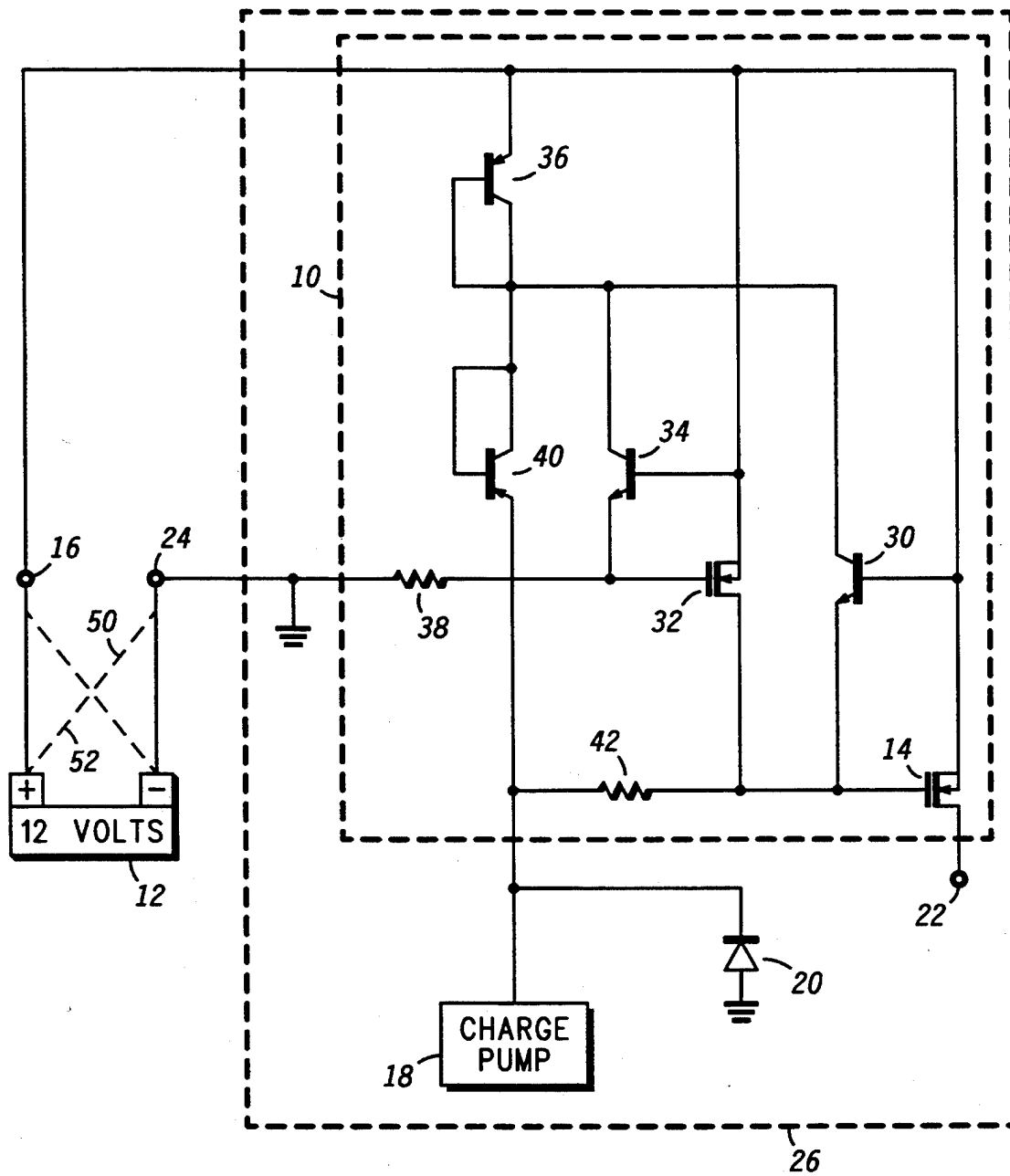
8 Claims, 1 Drawing Sheet



U.S. Patent

July 18, 1995

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REVERSE BATTERY PROTECTION CIRCUIT**FIELD OF THE INVENTION**

This invention relates to protection circuits and, in particular but not limited to, a reverse battery protection circuit for use in automotive applications.

BACKGROUND OF THE INVENTION

There currently exists a numerous types of electronic integrated circuits (IC's) for use in the automotive industry. Generally, the power supply for these circuits are generated from a 12-volt battery in an automobile. However, automotive IC's tied to the battery must survive the battery being hooked up backwards, for example, to avoid forward biasing epitaxial layers of the IC that are tied to the battery which thereby could result in destruction of the IC.

One attempt that prior art has made for providing reverse battery protection for IC's is to include a series diode between the battery and the integrated circuit wherein if the integrated circuit is connected to the battery backwards, the series diode is reversed biased and prevents supply voltage from being applied to the integrated circuit. However, the series diode solution compromises low voltage performance and the geometry of the diode becomes larger as supply current requirements increase.

Another attempt that prior art has made in providing reverse battery protection for an integrated circuit is to provide a saturated lateral PNP transistor in series between the battery and the integrated circuit. Although low voltage performance is not compromised in this solution, base current requirements for the lateral PNP increase power dissipation and the geometry of the PNP transistor becomes large as supply current requirements increase.

Another attempt that prior art has made in providing reverse battery protection for an integrated circuit is to provide a charged pumped reverse TMOS transistor as a pass device between the battery and the integrated circuit wherein the TMOS transistor has passive (resistive) gate to source termination. However, this solution requires DC current from the charge pump to enhance the TMOS transistor, and the turn off time of the TMOS transistor is limited by the size of the passive gate termination. Moreover, the charge pump must be high impedance when the supply voltage is reversed.

Hence, there exists a need for an improved reverse battery protection circuit for an integrated circuit that does not compromise low voltage performance, can efficiently handle moderate supply currents, does not demand DC current from a charge pump, and has a fast turn off time.

BRIEF DESCRIPTION OF THE DRAWING

The sole figure illustrates a detailed schematic diagram of a reverse battery protection circuit for protecting an integrated circuit in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWING

Referring to the sole figure, there is illustrated reverse battery protection circuit 10 fabricated within integrated circuit (IC) 26 and being coupled between battery 12 and terminal 22. It is understood that terminal 22 is further coupled to additional circuitry wherein this additional circuitry is desired to be protected from

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reverse battery hook up. IC 26 includes protection circuit 10 as well as charge pump 18, and any additional circuitry (not shown) coupled to terminal 22. Terminal 24 is coupled to a ground reference of IC 26.

Protection circuit 10 includes pass transistor 14 having a source electrode coupled to terminal 16 while the gate electrode of transistor 14 is coupled through resistor 42 to charge pump 18. The back gate of transistor 14 is coupled to the source electrode of transistor 14 while the drain electrode of transistor 14 is coupled to terminal 22.

Protection circuit 10 further includes transistor/zener diode 30 having a base coupled to terminal 16 and an emitter coupled to the gate electrode of transistor 14 and to the drain electrode of transistor 32. The collector of transistor 30 is coupled to the collectors of transistor/zener diode 34 and transistor/diode 36 wherein the collector of transistor 36 is coupled to its base. The emitter of transistor 36 and the base of transistor 34 are both coupled to terminal 16.

Moreover, the source electrode of transistor 32 and the back gate electrode of transistor 32 are coupled to terminal 16. The emitter of transistor 34 is coupled to the gate electrode of transistor 32 and returned to ground through resistor 38. The collector of transistor 34 is coupled to the collector of transistor/diode 40 wherein transistor 40 has its base coupled to its collector. The emitter of transistor 40 is coupled through resistor 42 to the gate electrode of transistor 14. Moreover, the emitter of transistor 40 is coupled to charge pump 18.

Charge pump 18 is coupled through diode 20 and returned to ground reference. In normal operation, transistor 14 requires the use of charge pump 18 to generate a voltage of at least 5 volts above a voltage supplied by battery 12. Moreover, charge pump 18 is typically available on IC 26 since it is required for other applications.

Under proper connection, the positive terminal of battery 12 is coupled to terminal 16 while the negative terminal of battery 12 is coupled to terminal 24. As a result, a positive supply voltage is applied to the source electrodes of transistors 32 and 14 as is desired. In this situation, transistor 14 is rendered operative while transistor 32 is rendered non-operative. As a result, the voltage appearing at terminal 22 (with respect to ground reference) will be substantially equal to the voltage appearing at terminal 16 (with respect to ground reference) less any IR drop occurring across transistor 14.

However, if battery 12 is improperly hooked up in a reverse manner wherein the positive terminal of battery 12 is coupled to terminal 24 while the negative terminal of battery 12 is coupled to terminal 16 as represented by dotted lines 50 and 52. This now means that a negative voltage (with respect to ground reference) is applied to the source electrodes of transistors 14 and 32 as is not desired. Under this condition, transistor 32 is rendered operative thereby shorting the gate electrode of transistor 14 to its source electrode and, thus, rendering transistor 14 non-operative. As a result, the voltage appearing at terminal 16 is not passed to terminal 22 and thus is not supplied to any additional internal IC circuitry. Further, any epitaxial layers typically coupled to terminal 22 cannot conduct current and damage integrated circuit 26.

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Transistor 30 functions as a zener diode to protect excessive voltage from appearing on the gate electrode of transistor 14. Essentially, the base of transistor 30 is the anode of the zener diode while the emitter of transistor 30 is the cathode of the zener diode. Moreover, the collector of transistor 30 is the third terminal of the zener diode and is coupled to the collector of transistor 34 which is the epitaxial island. Similarly, transistor 34 functions as a zener diode to protect excessive voltage from appearing on the gate electrode of transistor 32 wherein the base and emitters of transistor 34 respectively act as the anode and cathode of the zener diode while the collector of transistor 34 is coupled to the epitaxial island.

Moreover, resistor 38 functions to provide charge to render transistor 32 operative under a reverse battery condition. Also, resistor 42 functions to decouple the gate electrode of transistor 14 from charge pump 18.

It should be noted that components 30, 34, 32 and 38 are all fabricated in one epitaxial region which is biased by PNP transistors 36 and 40.

The present invention assures that no epitaxial islands are tied to terminal 16. As a result, if the connections of battery 12 are reversed, there are not epitaxial islands to be forward biased.

The present invention has several advantages. First, protection circuit 10 does not provide any additional DC loading on charge pump 18 when it is desired to enhance and turn on TMOS transistor 14. Second, under reverse battery conditions, charge pump 18 does not have to be heavily resistive or open for proper operation as is the case for prior art circuits. Thus, charge pump 18 does not have any special design requirements. Third, protection circuit 10 provides reverse battery protection without sacrificing power supply head room for low voltage operation since no series diodes are used. Moreover, the present invention quickly renders transistor 14 non-operative under a reverse battery condition. In particular, the discharge time constant for the gate electrode of transistor 14 is a product of the drain-source on resistance ($R_{DS(on)}$) of transistor 32 and the input capacitance (C_{ISS}) of transistor 14 which is substantially less than the turn off time for a passive gate termination scheme.

By now it should be apparent from the foregoing discussion that a novel protection circuit for protecting internal circuitry of an integrated circuit from a reverse battery connection has been provided. The protection circuit includes a pass transistor which is rendered operative when the supply voltage is properly connected to the integrated circuit. However, when the power supply is improperly connected, a second transistor becomes active thereby rendering the pass transistor inactive and not allowing the reverse supply voltage to be applied to the internal circuitry.

While the invention has been described in specific embodiments thereof, it is evident that many alterations, modifications and variations will be apparent to those skilled in the art. Further, it is intended to embrace all such alterations, modifications and variations in the appended claims.

I claim:

1. An integrated circuit having reverse battery protection, the integrated circuit including a charge pump and internal circuitry, the integrated circuit also including a protection circuit coupled between a first and second terminals wherein the first terminal is coupled to

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a battery and the second terminal is coupled to the internal circuitry, the protection circuit comprising:

a pass transistor having first and second current carrying electrodes and a control electrode, said first and second current carrying electrodes of said pass transistor respectively coupled between the first and second terminals, said control electrode of said pass transistor coupled to the charge pump;

a first transistor (32) having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said control electrode of said pass transistor, said second current carrying electrode of said first transistor coupled to the first terminal;

a second transistor (30) having a collector, a base and an emitter, said base of said second transistor being coupled to the first terminal, said emitter of said second transistor coupled to said first current carrying electrode of said first transistor;

a third transistor (34) having a collector, a base and an emitter, said base of said third transistor coupled to the first terminal, said emitter of said third transistor coupled to said control electrode of said first transistor, said collector of said third transistor coupled to said collector of said second transistor;

a fourth transistor (40) having a collector, a base and an emitter, said collector of said fourth transistor coupled to said collector of said third transistor, said base of said fourth transistor coupled to said collector of said fourth transistor, said emitter of said fourth transistor coupled to said control electrode of said pass transistor;

a fifth transistor (36) having a collector, a base and an emitter, said collector of said fifth transistor coupled to said collector of said fourth transistor, said base of said fifth transistor coupled to said collector of said fifth transistor, said emitter of said fifth transistor coupled to the first terminal; and

a first resistor (38) coupled between said control electrode of said first transistor and a first supply voltage terminal.

2. The protection circuit according to claim 1 further including a second resistor (42) coupled between said emitter of said fourth transistor and said control electrode of said pass transistor.

3. A circuit for protecting internal circuitry of an integrated circuit from reverse battery connection, the integrated circuit including a charge pump and having first and second terminals coupled to a battery for supplying power to the integrated circuit, the circuit comprising:

first means for passing a voltage appearing across the first and second terminals to the internal circuitry when the integrated circuit is properly connected to the battery, said first means coupled between the first terminal and the integrated circuit and coupled to the charge pump;

second means for rendering said first means non-operative when the integrated circuit is improperly connected to the battery thereby blocking said voltage appearing across said first and second terminals from being passed to the internal circuitry, said second means including a first transistor which is rendered operative when the integrated circuit is improperly connected to the battery, said second means coupled between the first terminal and said first means.

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4. The circuit according to claim 3 wherein said second means includes:

said first transistor (32) having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said first means, said second current carrying electrode of said first transistor coupled to the first terminal;

a second transistor (30) having a collector, a base and an emitter, said base of said second transistor coupled to the first terminal, said emitter of said second transistor coupled to said first current carrying electrode of said first transistor;

a third transistor (34) having a collector, a base and an emitter, said base of said third transistor coupled to the first terminal, said emitter of said third transistor coupled to said control electrode of said first transistor, said collector of said third transistor coupled to said collector of said second transistor;

a fourth transistor (40) having a collector, a base and an emitter, said collector of said fourth transistor coupled to said collector of said third transistor, said base of said fourth transistor coupled to said collector of said fourth transistor;

a fifth transistor (36) having a collector, a base and an emitter, said collector of said fifth transistor coupled to said collector of said fourth transistor, said base of said fifth transistor coupled to said collector of said fifth transistor, said emitter of said fifth transistor coupled to the first terminal;

a first resistor (38) coupled between said control electrode of said first transistor and a first supply voltage terminal; and

a second resistor (42) coupled between said emitter of said fourth transistor and said first means.

5. The circuit according to claim 3 wherein said second means includes:

a first transistor (32) having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said first means, said second current carrying electrode of said first transistor coupled to the first terminal;

first zener diode means (30) coupled across said second and control electrodes of said first transistor for limiting a voltage appearing thereacross; and bias means coupled between the first terminal and said first means for biasing an epitaxial region in

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which said first transistor and said first zener diode means are fabricated.

6. The circuit according to claim 5 wherein said second means further includes second zener diode means (34) coupled across said first means for limiting a voltage appearing thereacross, said second zener diode means also being fabricated in said epitaxial region.

7. A method for providing reverse battery protection to internal circuitry of an integrated circuit, the integrated circuit having first and second terminals for coupling to a battery, the method comprising the steps of:

allowing a voltage appearing at the first terminal to pass through a transistor to the internal circuitry when the integrated circuit is properly coupled to the battery; and

actively disabling said transistor when the integrated circuit is improperly coupled to the battery thereby preventing said voltage appearing at the first terminal to pass to the internal circuitry.

8. An integrated circuit having reverse battery protection, the integrated circuit including a charge pump and internal circuitry, the integrated circuit also including a protection circuit coupled between first and second terminals wherein the first terminal is coupled to a battery and the second terminal is coupled to the internal circuitry, the protection circuit comprising:

a pass transistor having first and second current carrying electrodes and a control electrode, said first and second current carrying electrodes of said pass transistor respectively coupled between the first and second terminals, said control electrode of said pass transistor coupled to the charge pump; and

a first transistor for actively disabling said pass transistor when the battery is improperly connected thereby preventing a voltage appearing on the first terminal from appearing at the second terminal, said first transistor having first and second current carrying electrodes and a control electrode, said first current carrying electrode of said first transistor coupled to said control electrode of said pass transistor, said second current carrying electrode of said first transistor coupled to said first current carrying electrode of said pass transistor, said control electrode of said first transistor coupled to ground reference.

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EXHIBIT F



US005776798A

United States Patent

[19]

[11] **Patent Number:** **5,776,798****Quan et al.**[45] **Date of Patent:** **Jul. 7, 1998**[54] **SEMICONDUCTOR PACKAGE AND METHOD THEREOF**

[75] Inventors: **Son Ky Quan**, Fountain Hills; **Samuel L. Coffman**, Scottsdale; **Bruce Reid**, Mesa; **Keith E. Nelson**, Tempe, all of Ariz.; **Deborah A. Hagen**, Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **708,296**

[22] Filed: **Sep. 4, 1996**

[51] Int. Cl.⁶ **H01L 21/44**

[52] U.S. Cl. **438/112; 438/460**

[58] Field of Search 438/112, 113, 438/460, 464, 465

[56] **References Cited****U.S. PATENT DOCUMENTS**

4,961,821 10/1990 Drake et al. 438/113
5,061,657 10/1991 Queen et al. 438/126

5,188,984 2/1993 Nishiguchi 438/125
5,462,636 10/1995 Chen et al. 438/465
5,491,111 2/1996 Tai 438/113
5,604,160 2/1997 Warfield 438/113
5,641,714 6/1997 Yamanaka 438/464

OTHER PUBLICATIONS

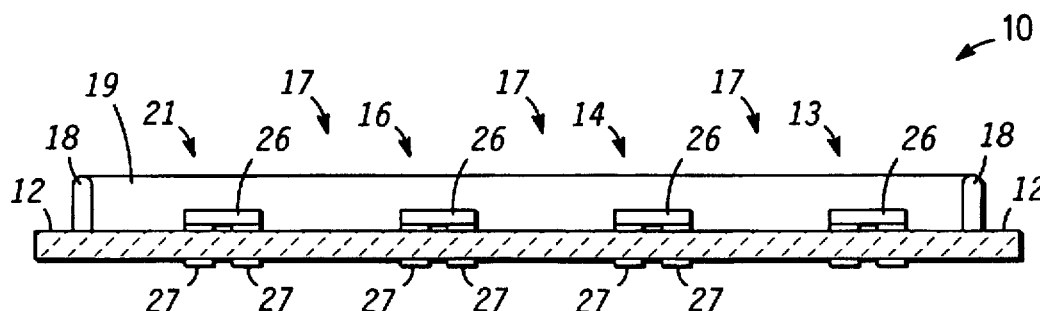
Arnold et al., "Stressed-out-Microelectronic Encapsulation Finds Cure in Aerobic Adhesives", Advanced Packaging, Jan./Feb. 1996, pp. 30,32,34.

Primary Examiner—Kevin Picardat

Attorney, Agent, or Firm—Robert F. Hightower

[57] **ABSTRACT**

A semiconductor package substrate (10) has an array of package sites (13,14,16,21,22, and 23) that are substantially identical. The entire array of package sites (13,14,16,21,22, and 23) is covered by an encapsulant (19). The individual package sites (13,14,16,21,22, and 23) are singulated by sawing through the encapsulant (19) and the underlying semiconductor package substrate (10).

12 Claims, 1 Drawing Sheet

U.S. Patent

Jul. 7, 1998

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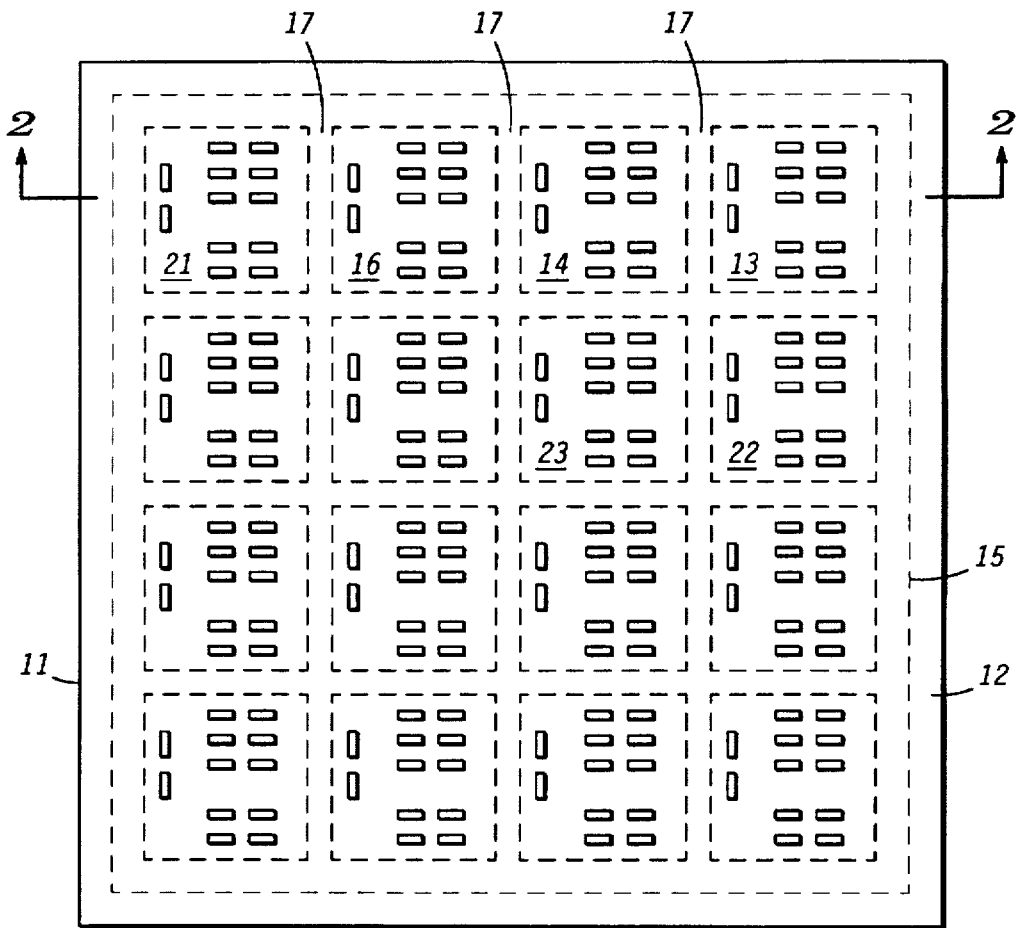


FIG. 1

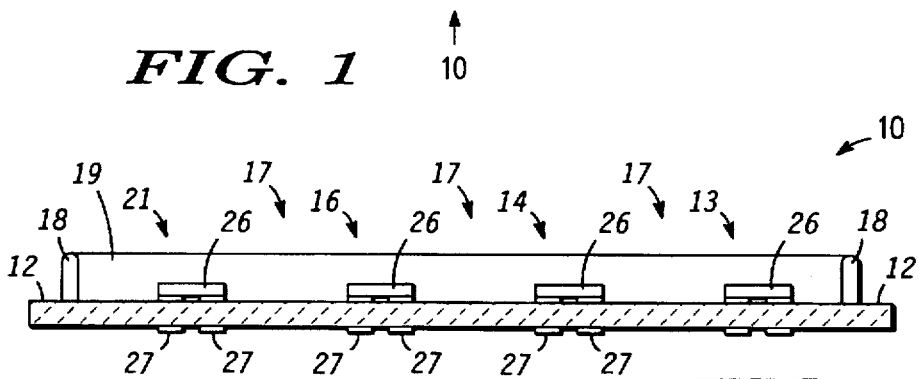


FIG. 2

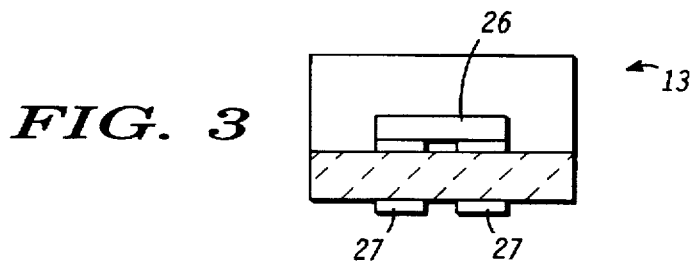


FIG. 3

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SEMICONDUCTOR PACKAGE AND METHOD THEREOF

BACKGROUND OF THE INVENTION

The present invention relates, in general, to packaging techniques, and more particularly, to a novel semiconductor package.

In the past, the semiconductor industry has utilized a variety of encapsulation techniques for forming the body of semiconductor packages. Typically, the semiconductor and other devices are assembled onto an interconnect platform or substrate such as a leadframe, printed circuit board or ceramic substrate. One particular encapsulating technique, commonly referred to as glob-top, involves dispensing an encapsulant to cover semiconductor devices or other components that are assembled onto the substrate. One problem with this prior technique is the planarity of the top surface of the encapsulant. Often, the top surface has a convex shape. Because of the convex shape, automated pick and place equipment can not utilize the resulting semiconductor package. Also, it is difficult to mark the top surface because of the convex shape.

Such techniques usually encapsulate a single assembly site on a substrate and after encapsulation, the assembly site is singulated to form an individual package. Consequently, assembly time and singulation time are long and result in high package cost.

Accordingly, it is desirable to have a semiconductor package that has a substantially planar surface that can be utilized with automated pick and place equipment, that is easily marked, and that increases throughput thereby reducing the cycle time and assembly costs.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a plan view of a semiconductor package at a stage of manufacturing in accordance with the present invention;

FIG. 2 illustrates a cross-sectional view of the package of FIG. 1 at a subsequent manufacturing stage; and

FIG. 3 illustrates a cross-sectional view of a singulated semiconductor package in accordance with the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 1 schematically illustrates an embodiment of a semiconductor package substrate or semiconductor package 10 at a stage of manufacturing. Package 10 includes an interconnect substrate 11 that has a plurality of package sites such as package sites 13, 14, 16, 21, 22, and 23. As will be seen hereinafter, each of sites 13, 14, 16, 21, 22, and 23 will subsequently be singulated into an individual singulated semiconductor package. Each of sites 13, 14, 16, 21, 22, and 23 are substantially identical and have areas within each site for attaching and interconnecting a plurality of electronic components such as active semiconductor devices, and passive elements such as resistors and capacitors. Each of sites 13, 14, 16, 21, 22, and 23 are separated by a space, for example space 17 between sites 16 and 21, so that each site may be singulated into an individual package.

Substrate 11 can have a variety of forms including a stamped leadframe, a ceramic substrate, a printed circuit board substrate, and other configurations that are well known to those skilled in the art. As shown in FIG. 1, substrate 11 is a ceramic substrate having multiple layers of electrical interconnect separated by dielectrics, and multiple attachment areas.

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Substrate 11 also includes a dam-bar area 12 around the periphery of substrate 11, thus, surrounding the periphery of the plurality of package sites as indicated by a dashed line 15. As will be seen hereinafter, dam-bar area 12 is used for encapsulating package 10 and individual packages formed by each package site of the plurality of package sites, such as sites 13, 14, 16, 21, 22, and 23.

FIG. 2 illustrates a cross-sectional schematic of package 10 at a subsequent stage of manufacturing and is taken along cross-sectional line 2—2 shown in FIG. 1. The same reference numbers are used to represent the same elements among the drawings. Typically, components such as semiconductor devices or passive elements are attached to each package site as illustrated by a component 26 attached to sites 13, 14, 16, and 21. Many components may be attached to each package site, device 26 is shown only for illustration purposes. As shown in FIG. 2, encapsulating each package site of the plurality of package sites and associated components includes forming a dam-bar 18 on area 12. Dam-bar 18 creates a cavity containing the plurality of package sites. Dam-bar 18 is formed by dispensing a first encapsulating material onto area 12. The first encapsulating material has a first viscosity that is sufficiently high so that the encapsulating material does not flow across substrate 11 but substantially remains as dispensed onto area 12. Typically, the first encapsulating material has a high viscosity that is greater than approximately 500,000 centi-poise (cps), and typically has a viscosity of 1,000,000 to 2,000,000 cps at approximately 25° C. (degrees Celsius). One suitable first encapsulating material for dam-bar 18 is a rigid thermosetting epoxy such as FP-4451 manufactured by Hysol-Dexter of Industry, Calif.

Generally, the first encapsulating material is heated during dispensing by heating the syringe or dispensing mechanism so that the first encapsulating material can be dispensed. Additionally, substrate 11 generally is also heated to a higher temperature so that the first encapsulating material flows sufficiently to form dam-bar 18. Generally, the dispensing mechanism or syringe is heated to approximately forty to fifty degrees Celsius (40°–50° C.), and substrate 11 generally is heated to approximately eighty to ninety degrees Celsius.

Thereafter, a second encapsulating material is dispensed within the cavity formed by dam-bar 18 to form an encapsulant 19 covering the components on substrate 11. The thickness of encapsulant 19 is sufficient to cover and protect components such as component 26 formed on substrate 11. The second encapsulating material has a second viscosity that is sufficiently low so that the second encapsulating material flows to fill the cavity leaving no voids and surrounds the components and attachment wires used to connect components to substrate 11. The second viscosity is less than the 500,000 cps high viscosity of the first encapsulating material and typically is approximately 20,000 to 200,000 cps at 25° C. One example of a suitable material for the second encapsulating material is FP-4650 manufactured by Hysol-Dexter. Additionally, the second encapsulating material typically has the same chemical base as the first encapsulating material so that the two materials bond at the interface to minimize separation and potential contamination. During dispensing, the second encapsulating material and substrate 11 are heated similarly to the heating used for dispensing the first encapsulating material.

After dispensing, the first and second encapsulating materials are heated to gel both encapsulating materials in order to control subsequent out gassing and warpage of substrate 11. Typically, both encapsulating materials are gelled for

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approximately one hour at one hundred ten degrees Celsius. Subsequently, dam-bar 18 and encapsulant 19 are cured so that encapsulant 19 forms a continuous encapsulating material covering the underlying components. Typically the curing is performed at a temperature of approximately 165° C. for a time of up to two hours. After curing, each individual package site is singulated into a singulated package by using space 17 for sawing completely through encapsulant 19 and substrate 11. For example, a ceramic saw is used to saw through encapsulant 19 and substrate 11 when substrate 11 is ceramic material. Other singulation techniques could be utilized including laser cutting through encapsulant 19 and substrate 11.

The area covered by encapsulant 19 should be larger than the meniscus formed by the second encapsulating material so that the top surface of encapsulant 19 remains substantially planar. For example, the top surface should have a deviation of less than plus or minus 0.13 millimeters across the surface of encapsulant 19. As shown in FIG. 2, the plurality of package sites are formed in an 4x4 array but could also be formed in other arrays. An array that is sixty by sixty millimeters provides a sufficient area to provide the desired planarity.

It should be noted that other encapsulating techniques could be utilized to cover the plurality of package sites with an encapsulating material in order to encapsulate package 10. For example, dam-bar 18 could be a premanufactured frame applied to area 12, and overmolding or other techniques could be used for the encapsulating. Thereafter each package site can be singulated as described hereinbefore.

FIG. 3 illustrates a cross-sectional view of a singulated package formed from a package site such as package site 13 shown in FIG. 1 and FIG. 2.

By now it should be appreciated that there has been provided a novel semiconductor package and method therefor. Forming a plurality of package sites on a substrate and using one dam-bar around the entire periphery surrounding the plurality of package sites, facilitates forming a substantially planar surface on the encapsulant. Forming a substantially planar surface allows each singulated package to have a substantially planar surface and facilitates utilization with automated pick and place equipment, and also facilitates clear marking of each singulated package. Forming the plurality of package sites adjacent to each other and covering the plurality of package sites with one continuous encapsulant minimizes space required to singulate the package sites and maximizes the number of package sites on a substrate thereby providing the smallest package outline and lowering package costs.

We claim:

1. A method of forming a semiconductor package comprising:

forming a substrate having a plurality of package sites and an electronic component attached to the plurality of package sites;

encapsulating the plurality of package sites wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites; and

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singulating through the encapsulating material to singulate each package site into an individual package.

2. A method of forming a semiconductor package comprising:

encapsulating a plurality of package sites that are on a substrate wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites and wherein encapsulating the plurality of package sites includes forming the encapsulating material to have a top surface planarity deviation of less than 0.13 millimeters; and

singulate through the encapsulating material to singulate each package site.

3. A method of forming a semiconductor package comprising:

encapsulating a plurality of package sites that are on a substrate wherein the encapsulating forms a continuous encapsulating material covering the plurality of package sites and wherein encapsulating the plurality of package sites includes forming a dam bar surrounding the periphery of the plurality of package sites for forming a cavity containing the plurality of package sites, and dispensing the encapsulating material within the cavity; and

singulating through the encapsulating material to singulate each package site.

4. The method of claim 3 wherein forming the dam bar includes dispensing a first encapsulating material having a first viscosity.

5. The method of claim 4 wherein dispensing the encapsulating material within the cavity includes dispensing a second encapsulating material having a second viscosity that is lower than the first viscosity.

6. The method of claim 5 wherein dispensing the first encapsulating material having the first viscosity includes having a viscosity of 1,000,000 to 2,000,000 cps.

7. The method of claim 5 wherein dispensing the second encapsulating material having the second viscosity includes having a viscosity less than 500,000 cps.

8. The method of claim 5 further including gelling both the first and second encapsulating materials prior to curing both the first and second encapsulating materials.

9. The method of claim 5 wherein dispensing the first encapsulating material includes heating the first encapsulating material.

10. The method of claim 5 wherein dispensing the second encapsulating material includes heating the second encapsulating material.

11. The method of claim 1 wherein singulating through the encapsulating material includes sawing through the encapsulating material and the substrate.

12. The method of claim 1 wherein encapsulating the plurality of package sites includes encapsulating by overmolding.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,776,798
DATED : July 7, 1998
INVENTOR(S) : Son Quan et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 4, claim 2, line 13, delete "singulate" and insert --singulating--.

Signed and Sealed this
Fifteenth Day of June, 1999

Attest:



Q. TODD DICKINSON

Attesting Officer

Acting Commissioner of Patents and Trademarks